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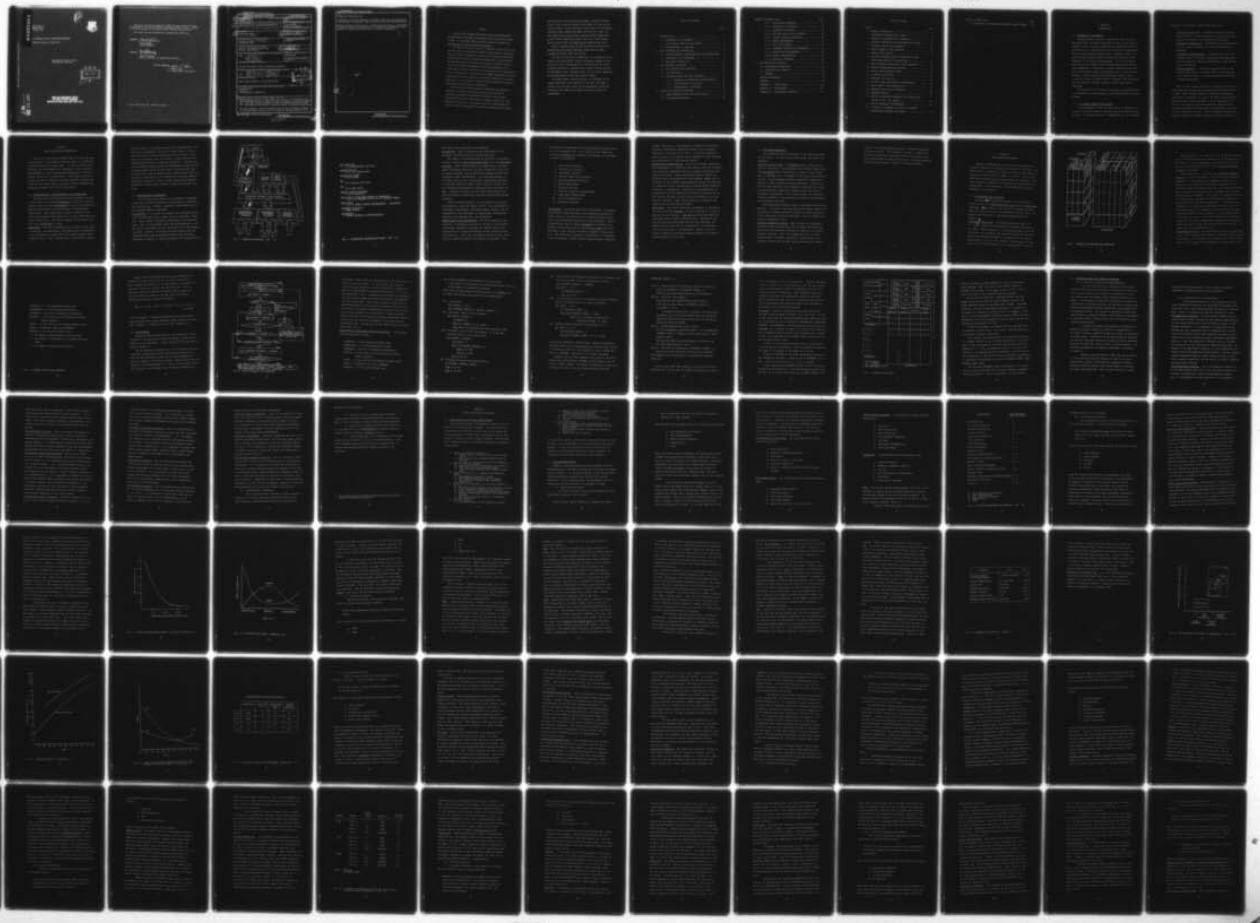

RADC-TR-77-28
Phase Report
January 1977

A COLLECTED GUIDE TO MICROSYSTEM SELECTION

Clarkson College of Technology

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
GRIFFISS AIR FORCE BASE, NEW YORK 13441

A COLLECTED GUIDE TO MICROSYSTEM SELECTION

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Microprocessors, because of their small size, low cost, and versatility, are being considered for use in areas classically unrelated to Electrical Engineering. Thus, many persons untrained in electrical engineering principles must face the problem of microprocessor selection without the necessary background.

The report presents a selection algorithm and the basic information required by this algorithm to allow the novice to grasp the concepts required of him

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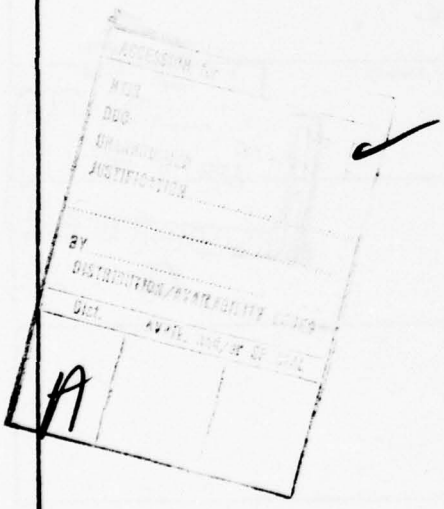
during the selection process.

In addition, the role of computers in creating a data base, and operating on this data base is discussed. Ideas for future work in the area are generated.

Finally, material concerning where to find microsystem vendors, a bibliography of published material on microprocessors, microprocessor descriptions, and a glossary of commonly used terminology is included as appendices.



PREFACE

This effort was conducted by Clarkson College of Technology under the sponsorship of the Rome Air Development Center Post-Doctoral Program for DMA. Mr. David Trad, RADC/IS, was the task project engineer and provided overall technical direction and guidance.

The RADC Post-Doctoral Program is a cooperative venture between RADC and some sixty-five universities eligible to participate in the program. Syracuse University (Department of Electrical and Computer Engineering), Purdue University (School of Electrical Engineering), Georgia Institute of Technology (School of Electrical Engineering), and State University of New York at Buffalo (Department of Electrical Engineering) act as prime contractor schools with other schools participating via sub-contracts with the prime schools. The U.S. Air Force Academy (Department of Electrical Engineering), Air Force Institute of Technology (Department of Electrical Engineering), and the Naval Post Graduate School (Department of Electrical Engineering) also participate in the program.

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Space and Missile Systems Orgarization (SAMSO), Aeronautical Systems Division (ASD), Electronic Systems Division (ESD), Air Force Avionics Laboratory (AFAL), Foreign Technology Division (FTD), Air Force Weapons Laboratory (AFWL), Armament Development and Test Center (ADTC), Air Force Communications Service (AFCS), Aerospace Defense Command (ADC), Hq USAF, Defense Communications Agency (DCA), Navy, Army, Aerospace Medical Division (AMD), and Federal Aviation Administration (FAA).

Further information about the RADC Post-Doctoral Program can be obtained from Jacob Scherer, RADC/RBC, Griffiss AFB, NY, 13441, telephone AV 587-2543, COMM (315) 330-2543.

The author of this report is Thomas Cole. He received his B.S.E.E. degree in 1975 from Clarkson College of Technology, Potsdam, New York. From 1975 to 1976 he was employed as a Research Assistant at Clarkson College of Technology in connection with a contract from DMA and Rome Air Development Center. Beginning in June, 1976, he will be employed as an Associate Engineer at IBM, Essex Junction, Vermont.

The author wishes to thank his advisor, Dr. David Bray, for his support and guidance in the completion of this work. The author is grateful also to his wife, Ellen, for her perseverance in typing and retyping the many drafts of this paper; and for her interest and encouragement.

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CHAPTER 1

INTRODUCTION

1.1 STATEMENT OF THE PROBLEM

Microprocessors, because of their small size, low cost, and versatility, are being considered for use in many areas of industry. This is forcing engineers and managers of diverse disciplines to be concerned with the selection of microprocessors for their specific applications. Presently, there is no guide available which presents a structured approach to the selection of the proper microprocessor. It is particularly difficult for the novice in the microprocessor field because most information is scattered in product brochures which tend to be restricted in scope, unreferenced, and of limited availability. Journal articles are beginning to appear, but as in any new field the subject matter is diverse, the definitions are not standard, and many important subjects are not yet discussed.

The purpose of this report is to present a proposed selection technique to aid engineers in the microprocessor selection process.

1.2 THE APPROACH TAKEN BY THIS REPORT

A basic premise of this work was that it is essential to establish a form of order to the many aspects of the selection process. It is believed that to accomplish this, four problem

areas must be addressed. Specifically these are:

Information collection. Information must be collected under one cover so that the selector's time may be used studying the material, not gathering the material.

Information presentation. Information must be presented in a way useful to persons of varied backgrounds and knowledge.

Information maintainability. Information must be maintainable, that is, deleting old material and adding new material should not require reorganization, just require simple bookkeeping.

Selection process. A structured procedure must be developed which defines, in proper order, the attributes to be taken to select the proper microprocessor for the intended application.

Each of these problem areas are considered in this report. First presented are the basic concepts and terminology which are used. Then a formal selection algorithm is presented, followed by a discussion of each of the chosen microprocessor attributes used in the algorithm. For the information collection, presentation, and maintainability problem areas, a suggested framework for cataloguing microprocessors according to their properties is given. Also, a suggested scheme for a computer program to automate the selection process (and as a

means of maintaining a microprocessor data base) is presented.

1.3 CONTRIBUTIONS OF THIS WORK

The principle contributions of this work can be summarized as follows:

1) A specific selection algorithm has been proposed for the purpose of proper microprocessor selection.

2) A large volume of separately published material has been collected, ordered, and presented in one report.

3) Suggestions for future work in the areas of refining microprocessor selection techniques using computer analysis, standardization of microprocessor interfaces, and the universal microprocessor concept have been advanced.

The specific selection algorithm and the collected information contained within this report are designed to serve as a background and guide for the newcomer in the field, and a reference to those with experience. It shows what to look for in a microprocessor, and the consequences of each choice. Thus, this report should contribute towards a better understanding of microprocessors by someone who uses microprocessors, designs new microprocessors, or wants to learn about microprocessors.

The suggestions for future work contained at the end of this report are presented with the hope that they will contribute in some measure to an eventual unified approach to the

design of microprocessor chips. The direct result of an eventual unified design approach would be making the selection process less one of gathering and documenting hundreds of different microprocessors, and more one of choosing from among a small set of different architectures.

CHAPTER 2

BASIC CONCEPTS AND TERMINOLOGY

There is an uncertainty generated when one uses the term microprocessor or microcomputer because there is no generally accepted definition of these ideas. To some the words microprocessor and microcomputer are synonomous, while to others a microcomputer is just a specialized application of the more general concept of a microprocessor. This chapter serves to clarify the use of several of the more important concepts and terms in this report, while a glossary of other commonly used terminology appears at the end of the report.

2.1 MICROPROCESSORS, MICROCOMPUTERS, AND MICROSYSTEMS

When the terms microprocessor and microcomputer are used in this report, the term microprocessor is used as a general concept, while the term microcomputer is used to indicate the specific application of microprocessors to computer-like applications. This terminology is used to stress the fact that microprocessors find application in areas other than computer oriented ones. More often, however, an even more general term, microsystem, is used.

Microsystem. The term microsystem will be used in this report to represent a microprocessor, microcontroller, microcomputer, or any combination of these with other special-purpose semiconductor chips. Thus, a microsystem is considered to cover a

very wide range of integrated circuit (IC) architectures. The most basic microsystems are made of a small number of chips containing one to thirty integrated circuits forming, for example, an arithmetic logic unit (ALU), or some registers and interconnective buses, or some type of control. The most complex microsystems might perform as minicomputers consisting of a single board on which is positioned a microprocessor chip with auxiliary chips of memory, direct memory access (DMA) interfacing, input/output (I/O) interfacing, and other minicomputer-like functions. Figure 1 shows a typical microsystem, and Figure 2 shows typical ranges of these microsystems' features.

2.2 DEFINITION OF AN ALGORITHM

In this section the notion of an algorithm is presented along with an informal definition of the selection algorithm and its data base. Chapter 3 presents a formal definition of the proposed selection algorithm.

An algorithm. D. E. Knuth [17] defines the requirements that a set of rules must have in order to be an algorithm. These are: input, output, finiteness, definiteness, and effectiveness. They are requirements which can be interpreted to fit any form of algorithm, and are, of course, met in the proposed algorithm. However, to provide some more insight into the reasoning behind the Microsystem Selection (MS) Algorithm presented in Chapter 3, these requirements are reinterpreted in

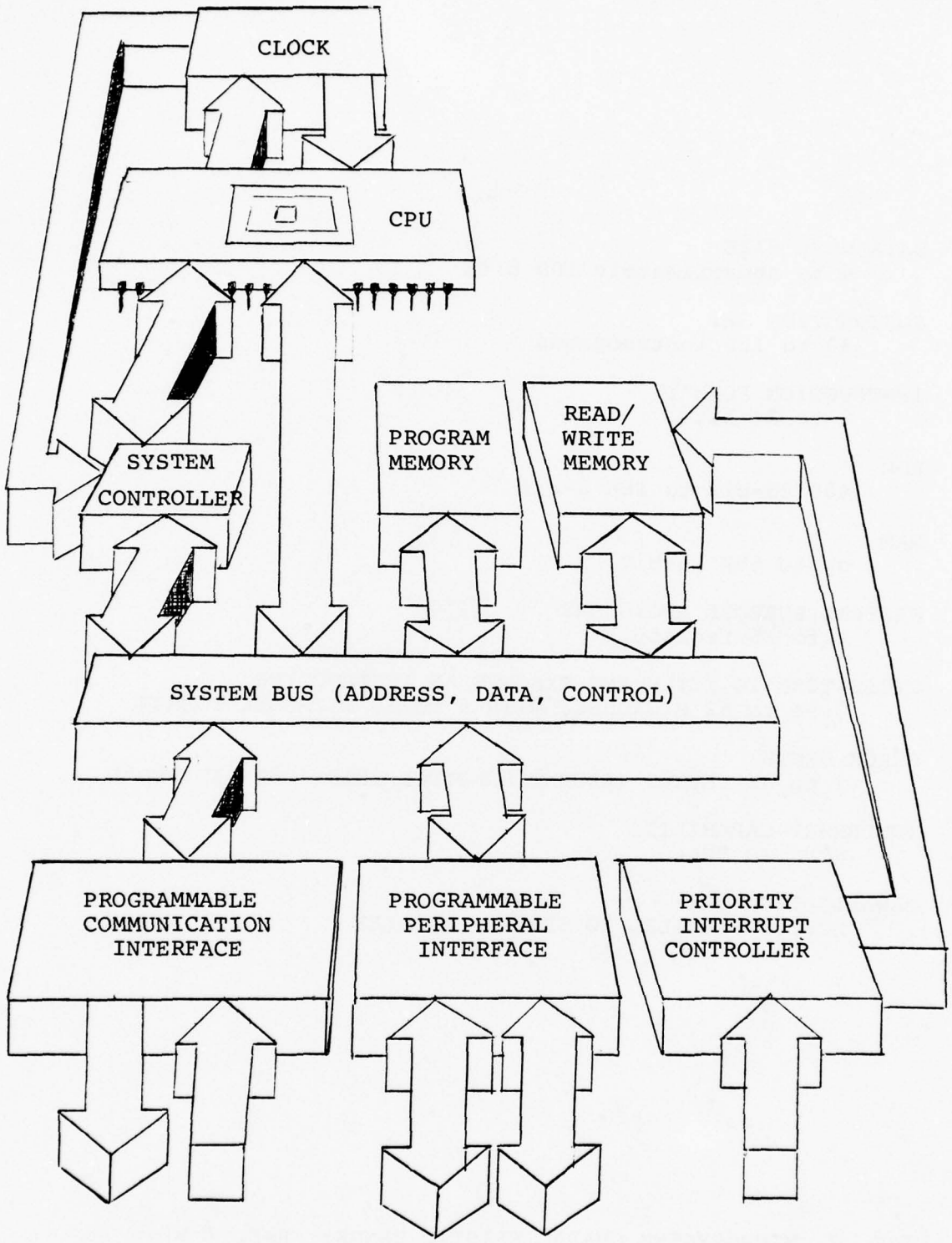


FIG. 1 EXAMPLE MICROSYSTEM: Ref. [3]

DATA WORD SIZE
4 to approximately 100 bits

INSTRUCTION SET
40 to 120 instructions

INSTRUCTION FORMAT
8 to 24 bits

ROM
400 23-bit to 16K 8-bit

RAM
up to 65K 16-bit

GENERAL PURPOSE REGISTERS
1 to 16 registers

CYCLE TIME TO FETCH AND EXECUTE AN INSTRUCTION
0.54 to 62 MICROSEC, WITH 5 to 10 MICROSEC COMMON

STACK DEPTH
2 to 32 LEVELS (RECENT ANNOUNCEMENTS: "UNLIMITED")

INTERRUPT CAPABILITY
NONE TO FULL

PARALLELISM
MOSTLY PARALLEL TO SERIAL/PARALLEL

FIG. 2 MICROSYSTEM CHARACTERISTIC RANGE: Ref. [9]

the light of the algorithm to be presented.

MS Algorithm. Before considering the requirements for an algorithm, the MS Algorithm is stated informally.

The inputs to the MS Algorithm are the user's requirement listing, called the desired-attribute table, and the microsystem data base. These inputs consist of, respectively, the microsystem attributes desired by the user (presented in the priority order selected), and the collected information about each microsystem under consideration. The algorithm operates on this data base by taking each required microsystem attribute in order and creating a master 'mask' which is 'placed over' all contending microsystems to determine which ones match the mask. Produced as output are only those microsystems which have successfully matched each and every required microsystem attribute.

From the above discussion, one can easily see that the requirements of input and output are met. The requirements of finiteness, definiteness, and effectiveness, however, are reinterpreted to the principles of completeness, definiteness, modularity and modifiability, and reliability.

Completeness of the presentation. The first principle, completeness, is defined as the need to include in the selection process all information necessary for choosing the correct microsystem for a particular design, without including extraneous material. Great care was taken to review as many journal articles, product brochures, and manuals as possible. Also,

interviews were conducted with various persons with experience in the microsystems field. As a result of this study, the following attributes are presented as necessary and sufficient to select a microsystem:

1) Application Criterion
2) Availability Criterion
3) Technology Criterion
4) Chip-Set Family Size Criterion
5) Software Analysis Criterion
6) Memory Requirements
7) Bus Size Criterion
8) Interrupt Capability Requirements
9) Power Supply Requirements
10) Timing Considerations
11) Low-Level Synthesis

Definiteness. The second principle, definiteness, is defined as the need to have each step of the algorithm precisely defined. That is, the actions to be carried out must be rigorously and unambiguously specified for each attribute. This is accomplished in part by naming attributes in relatively non-technical terminology, and by providing key values under each attribute to help identify the action required at that point. (e.g. The second major attribute, Availability, is subdivided into five sections: Double Sourced, Single Sourced, Threshold,

Planned, and Future.) Definiteness is placed in its relative position to stress the importance placed on using language familiar to a majority of the users. A very real attempt is made to replace the technical jargon appearing in many articles with terminology of a more general nature.

Modularity and modifiability. The third principle, modularity and modifiability, is defined as the need to order the attribute into relatively independent parts, or modules, which have well-defined interfaces. Having each module operate without assumptions about the operation of other modules, except what is contained in the interface specifications, allows the algorithm to incorporate future restructuring as simple module additions, deletions, or reorderings. Modularity and modifiability are incorporated into the selection algorithm by starting with the most general attribute and selectively proceeding to the most specific attribute. Thus, each attribute is completely subsumed by all the previous attributes.

Reliability. The fourth principle, reliability, is defined as the need to prevent failures, or faulty selections, as well as recover from any failures. Failures are situations where the algorithm fails to report anything at all. Reliability can only be built into algorithms from the very beginning, not added on at the end; thus its consideration is established before starting work on the algorithm. However, final reliability tests and efficiency measures should be included in future endeavers in this area.

2.3 DATA BASE TERMINOLOGY

The discussion above has referred to the terms attribute and key values. In this section these terms, and others, are discussed.

Attribute and key value. An attribute names a specific feature, or attribute, of microsystems and is further broken down into key values which clearly define actions or ideas which must be selected from. An example of key values was presented earlier. The Microsystem Selection Algorithm is designed to operate on these carefully selected attributes. During each cycle of the algorithm a new attribute is selected to be used as a specification template to further narrow the field of contending microsystems. After careful study, the attributes listed in section 2.2 are proposed as necessary and sufficient for microsystem selection.

These attributes have been used to modularize the selection process. It is easy to add user-defined attributes, delete old attributes, or change attribute priority by simple alteration of the input list of desired attributes. This is studied more closely in Chapters 4 and 5.

Attribute selection function. When the user has determined which key values are desirable for his design, he enters his choices into the selection algorithm by means of an attribute selection function. This is an expression which is used to condense bulky, multipart information. Specifically, each attribute used by the algorithm may have the various combina-

tions of its key values identified by a particular attribute selection function. This expression is used to compare the various microsystems to determine those which conform to the users requirements and those which do not. Attribute selection functions are discussed in detail in the next chapter.

CHAPTER 3

THE SELECTION ALGORITHM

Chapter 2 presented the notion of an algorithm and an informal definition of the MS Algorithm and its data base. In this section is presented a formal definition of the proposed selection algorithm with an example of its use. First, the basic data structure used by the algorithm is presented. This data structure is abstract in the sense that a particular implementation is not presented. Only the contents and basic organization are defined.

3.1 MS ALGORITHM DATA STRUCTURE

The proposed MS Algorithm operates on two major user-defined inputs, the desired-attribute table and the microsystem data base. These tables, plus a list of contending microsystems, and various pointers, are discussed in detail below. An example data structure is presented diagrammatically in Figure 3.

Desired-attribute table. The desired-attribute table is a N x 3 table, where N is the number of attributes contained in the table. Table position (I, 1) contains the name of the I^{th} attribute to be considered and indirectly specifies the priority of the attribute by means of its position in the table. Specifically, it has the I^{th} priority. The attribute in position (1,1) has first priority, (2,1) second priority, and so

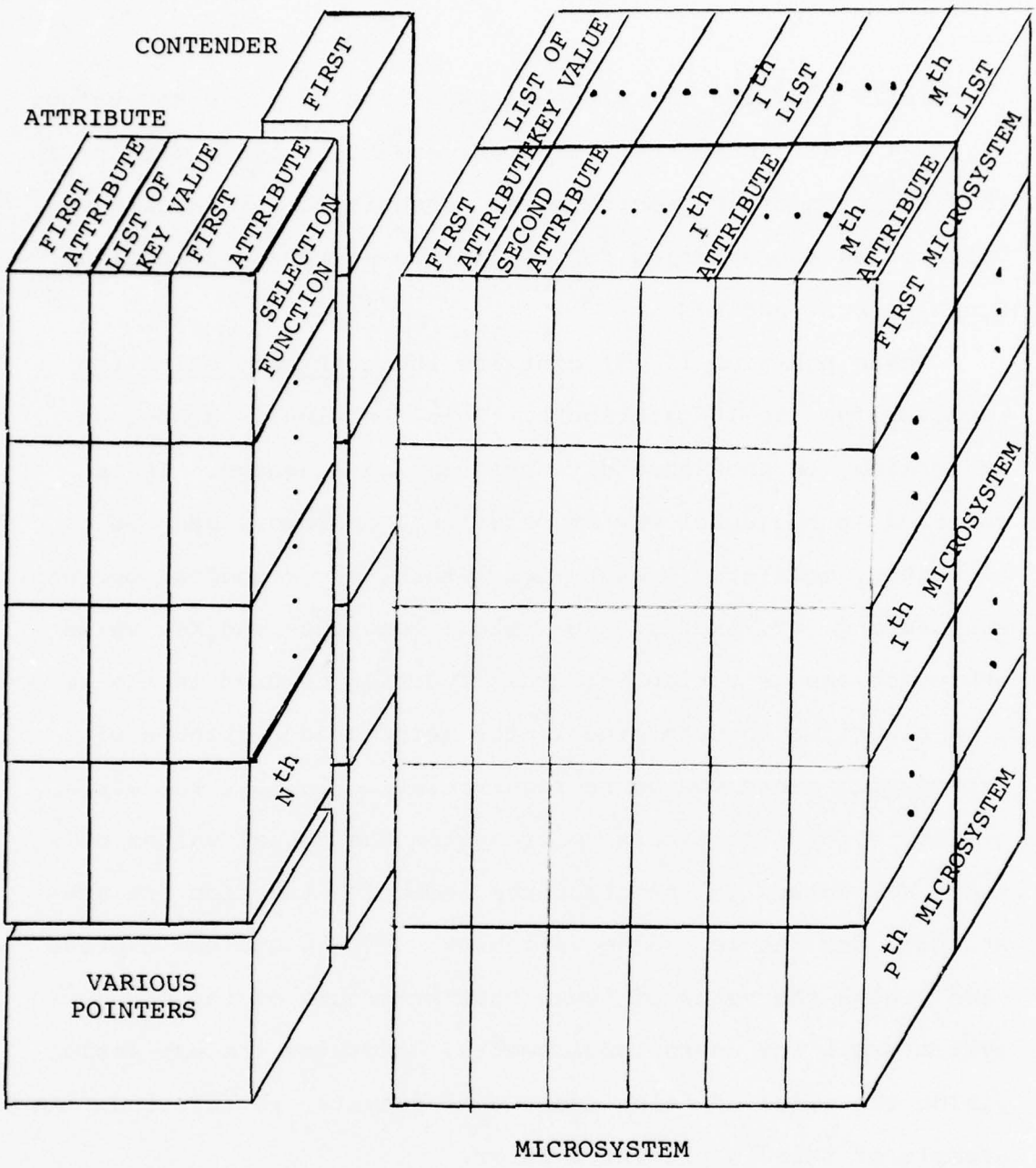


FIG. 3 EXAMPLE MS ALGORITHM DATA STRUCTURE

on.

Table position (I, 2) contains a list of those key values of the I^{th} attribute the user considers to be of importance in the selection of the microsystem. Associated with each key value is an abbreviation for use in the attribute selection function next defined.

Table position (I, 3) contains the attribute selection function for the I^{th} attribute. This function is a Boolean expression, in the sense of a programming language. It is composed in the usual way of relational operators such as less-than, equal-to, greater-equal-than, etc.; Boolean operators such as and, or, exclusive-or, etc.; constants and key value abbreviations as variables. This function is used in the selection algorithm to determine if the associated attribute of a microsystem meets the users requirements. To test the given attribute for a particular microsystem the actual values of those key values in the attribute selection function are substituted for the key value variables. If the Boolean expression yields the value of true, that attribute of the microsystem meets the users requirements; otherwise the expression yields the value of false and the microsystem is rejected. An example of this is presented later.

Microsystem data base. The microsystem data base contains data on all of the attributes and their key values for every possible microsystem. This data base is organized as a P x M x 2 table where P is the number of microsystems in the data base, and M

is the maximum number of attributes stored for any microsystem. In a similar manner to the desired-attribute table for microsystem K, table position (K, J, 1) names the J^{th} attribute. Position (K, J, 2) contains a list of all of the key values of the J^{th} attribute and has an associated value for each.

The set of proposed attributes and associated key values are presented in Figure 4. This list is believed to be a necessary and sufficient set of attributes for microsystem selection. As such the microsystem data base should contain data on each of these attributes for each possible microsystem. This position is defended in section 3.3.

Contender list. The last table needed by the MS Algorithm is the contender list. This is a P x 1 table where P is the number of microsystems in the data base. It is initialized to contain the indices of all microsystems and is restructured as each attribute is considered to contain only those microsystems which are still contenders for the desired microsystem.

The final elements of the data structure are pointers used by the algorithm. They are defined in the algorithm statement, and presented in Figure 5.

Example of the attribute selection function. Referring to Figure 4, it is noted that the key values of the availability attribute are: double sourced products, single sourced products, threshold products, planned products and future products. An example of an attribute selection function for this attribute is described next.

ATTRIBUTE	KEY VALUES
1) Application Criterion.....	Data Acquisition and Control Data Communications Human Interface Equipment Computational Other
2) Availability Criterion.....	Double Sourced Single Sourced Threshold Planned Future
3) Technology Criterion.....	PMOS NMOS CMOS IIL TTL OTHER (SOS, etc.)
4) Chip-Set Family Size.....	Single Chip CPU Bit Slice Divided-Function Chip-Set Single Board Computer (Kits) Single Chip Computer
5) Software Analysis Criterion.	Resident Assembler Cross Assembler Monitor High Level Language Instruction Simulator Prototyping System Special Instructions
6) Memory Requirements.....	Type/Size Microprogrammable DMA Asynchronous Operation
7) Bus Size Criterion.....	Four-Bits Eight-Bits Sixteen-Bits Other Sizes (12-, 32-bits)
8) Interrupt Capability.....	Single-Line Interrupt Multilevel Interrupt Vectored Interrupt No Interrupt
9) Power Supply Considerations.	Regulation & voltages required Environmental considerations
10) Timing Consideration.....	Frequencies Phase Circuit Quality
11) Low-Level Synthesis	

FIG. 4 PROPOSED ATTRIBUTES AND ASSOCIATED KEY VALUES

ATTRIBUTE -- is the desired-attribute table

MICROSYSTEM -- is the microsystem data base

CONTENDER -- the list of contending microsystems

MSINDEX -- is the index to the microsystem currently under evaluation

AINDEX -- is the index to the desired-attribute table

INDEX -- a temporary index into CONTENDER

EVALUATE -- is a function defined later

P -- the number of microsystems in the data base

N -- the number of attributes in the desired attribute table

M -- the number of microsystem attributes

FIG. 5 POINTERS USED BY THE ALGORITHM

Suppose that the abbreviations for the availability attribute key values are DS, SS, TP, PP and FP respectively. Also, suppose the symbols +, *, LT are chosen to represent the operators logical OR, logical AND, and less-than. Then an attribute selection function G involving some of these key values and the key values of cost and vendor reputation, abbreviated $ and VR, could be defined as:

G(DS, SS, $, VR) = (DS * ($ LT 100)) + (SS * (VR GT 5) * ($ LT 200))

G has the meaning: double sourced costing less than $100 or single sourced from a high reputation vendor costing less than $200 (assuming 5 is defined to be of 'high reputation').

3.2 THE ALGORITHM

Before the formal presentation of the algorithm, a brief abstract of its operation is given to provide a better understanding of the procedure. A block diagram of the algorithm is shown in Figure 6.

The MS Algorithm evaluates each of the attribute selection functions, representing the key value options chosen by the user for each included attribute for the microsystems in a priority ordering of the user's choice. Those microsystems conforming to the requirements (i.e. have a true attribute selection function) are retained, while those not conforming are

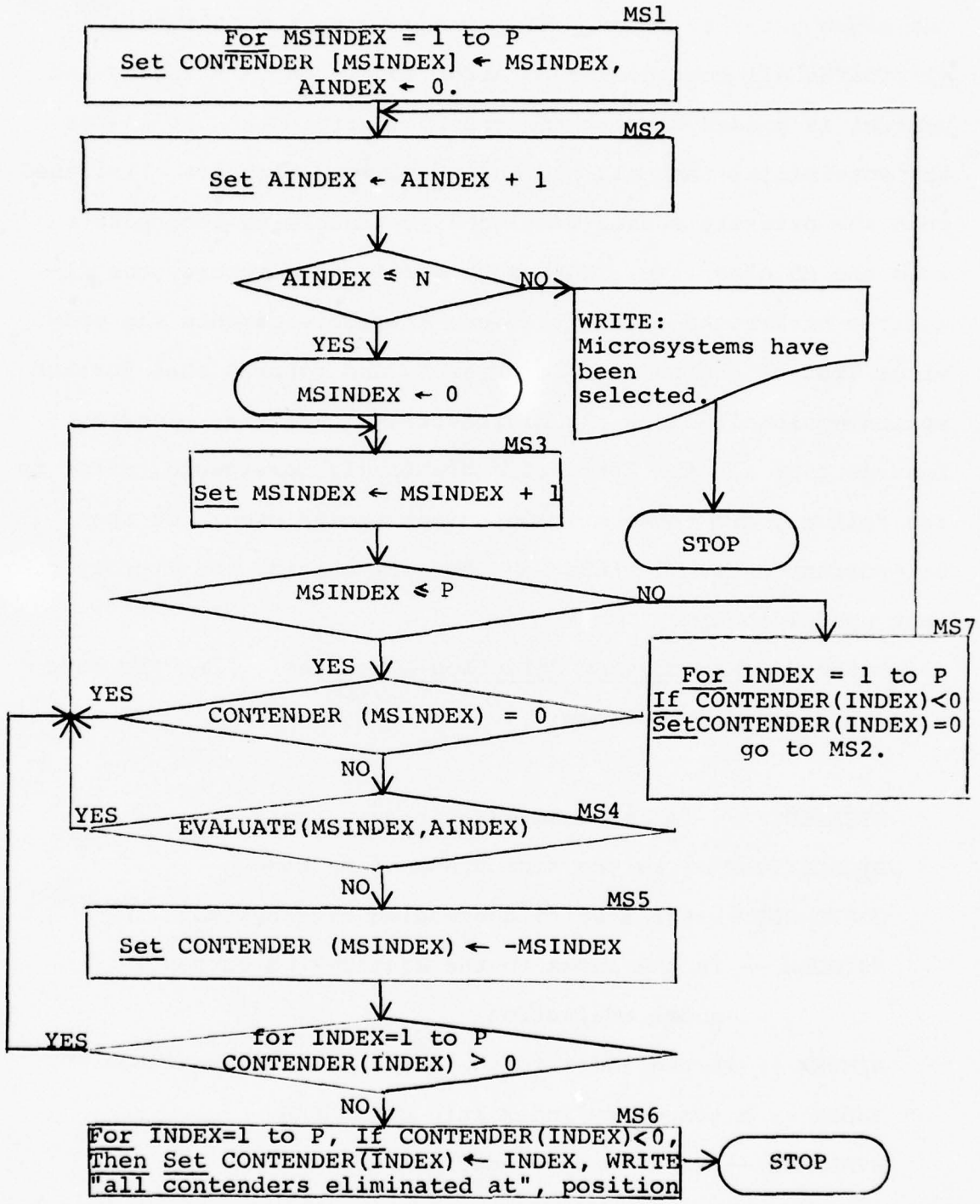


FIG. 6 BLOCK DIAGRAM OF THE ALGORITHM

eliminated. This action is repeated for all the attributes in the given priority order. If, at any time, the attribute eliminates all contenders; an error condition is flagged, and control is passed back to the previous attribute. It is for the possibility that all contending microsystems are eliminated that the priority scheme mentioned previously is incorporated into the MS Algorithm. When such a situation occurs, the algorithm backtracks to the previous attribute, prints the previous list of contending microsystems and reports that further action would eliminate all microsystems. Priority ordering insures that all the attributes previously considered, prior to the failure, are those most important to the user; not the unimportant ones. In this way the user obtains the microsystem most useful to him.

Algorithm MS (Microsystem Selection Algorithm). Let the data base be defined as follows:

ATTRIBUTE -- is the desired-attribute table
MICROSYSTEM -- is the microsystem data base
CONTENDER -- the list of contending microsystems
MSINDEX -- is the index to the microsystem currently under evaluation
AINDEX -- is the index to the desired-attribute table
INDEX -- a temporary index into CONTENDER
EVALUATE -- is a function defined later

Let P be the number of microsystems in the data base,

N the number of attributes in the desired attribute table and

M the number of microsystem attributes.

When the algorithm ends, the non-zero entries of CONTENDER will be those microsystems which meet the users requirements.

MS1 [Initialize.]

For MSINDEX = 1 to P

Set CONTENDER [MSINDEX] ← MSINDEX, AINDEX ← 0.

MS2 [Increment index to next attribute.]

Set AINDEX ← AINDEX + 1

If AINDEX ≤ N

Then Set MSINDEX ← 0, go to MS3

Else WRITE "Microsystems have been selected", STOP.

MS3 [Increment index to next microsystem. If it has been eliminated skip to next microsystem.]

Set MSINDEX ← MSINDEX + 1

If MSINDEX ≤ P

Then If CONTENDER (MSINDEX) = 0

Then go to MS3

Else go to MS4

Else go to MS7.

MS4 [Evaluate attribute selection function.]

If EVALUATE (MSINDEX, AINDEX)

Then go to MS3

Else go to MS5.

```
MS5  [Mark current microsystem to be deleted as a contender and
     test to determine if some contenders still exist.]
     Set CONTENDER (MSINDEX) ← -MSINDEX
     For INDEX = 1 to P
          If CONTENDER (INDEX) > 0
          Then go to MS3.
MS6  [All contenders have been eliminated by current attribute.
     Restore contenders prior to current attribute.]
     For INDEX = 1 to P
          If CONTENDER (INDEX) < 0
          Then Set CONTENDER (INDEX) ←  INDEX,
                    WRITE "all contenders eliminated at",
                         ATTRIBUTE (AINDEX, 1), STOP.
MS7  [Remove marked contenders from contender list.]
     For INDEX = 1 to P
          If CONTENDER (INDEX) < 0
          Then Set CONTENDER (INDEX) ← 0, go to MS2.
```

The function EVALUATE is defined next. Because the desired-attribute table and the microsystem data base have been defined on an abstract level it is not possible to give a formal definition of EVALUATE. Therefore it is defined informally.

EVALUATE has two input arguments, the index of the microsystem under consideration, MSINDEX, and the index of the desired attribute, AINDEX. The output of EVALUATE is either true or false, the value of the attribute-selection function,

ATTRIBUTE (AINDEX, 3).

Step 1) [Find those key values whose values are required.]

Scan the expression of ATTRIBUTE (AINDEX, 3).

Find all key value abbreviations in the expression.

Step 2) [Find key value names.]

For each key value abbreviation found in Step 1, find the key value names in ATTRIBUTE (INDEX, 2), for INDEX = 1 to N.

It should be noted that, in general, all microsystem attributes will have to be scanned since the attribute-selection function may contain key values of attributes other than those of AINDEX.

Step 3) [Search microsystem for key values.]

For all microsystem attributes INDEX = 1 to M MICROSYSTEM (MSINDEX, INDEX, 2) compare the key value names to those found in Step 2.

For each key value thus found assign its value to the key value abbreviation of Step 1.

Step 4) [Evaluate the expression of ATTRIBUTE (AINDEX, 3).]

Return the value thus found as the value of EVALUATE.

This completes the definition of the microsystem selection algorithm.

As in a pert chart type analysis, it may be said of this algorithm that, by the time one gathers the material to input

to the algorithm the work is already done. However, the sheer mass of information on each microsystem, and the ever growing number of microsystems, makes the bookkeeping the most time consuming portion of selection. This algorithm, therefore, attempts to automate the bookkeeping portion of selection, while assigning the user the task of evaluating his specific design requirements and presenting them to the algorithm as prescribed in the selection attributes.

An example. Consider a microsystem data base and desired attribute table as shown in Figure 7 to be the input. It can be seen that there are five microsystems under contention, with four attributes to use for selection (AVAILABILITY, TECHNOLOGY, SOFTWARE, and INTERRUPT). The MS Algorithm first sets up the CONTENDER list (as shown in Figure 7) to contain the index into each microsystem; and initializes the attribute index, AINDEX, to zero. The algorithm is now ready to begin cycling through the desired-attribute table.

In MS2, go to the first attribute found in the desired-attribute table, Availability. Noting the AINDEX is less than the number of attributes in the table, N; go to MS3.

In MS3, set MSINDEX to the first microsystem; and noting that MSINDEX is less than P, check to see if CONTENDER (1) is zero. Since it is not zero (it is a +1), go to MS4.

In MS4, perform the EVALUATE function on the first microsystem-first attribute pair. From the desired-attribute table one notes he is looking for the key value DOUBLE SOURCED. The

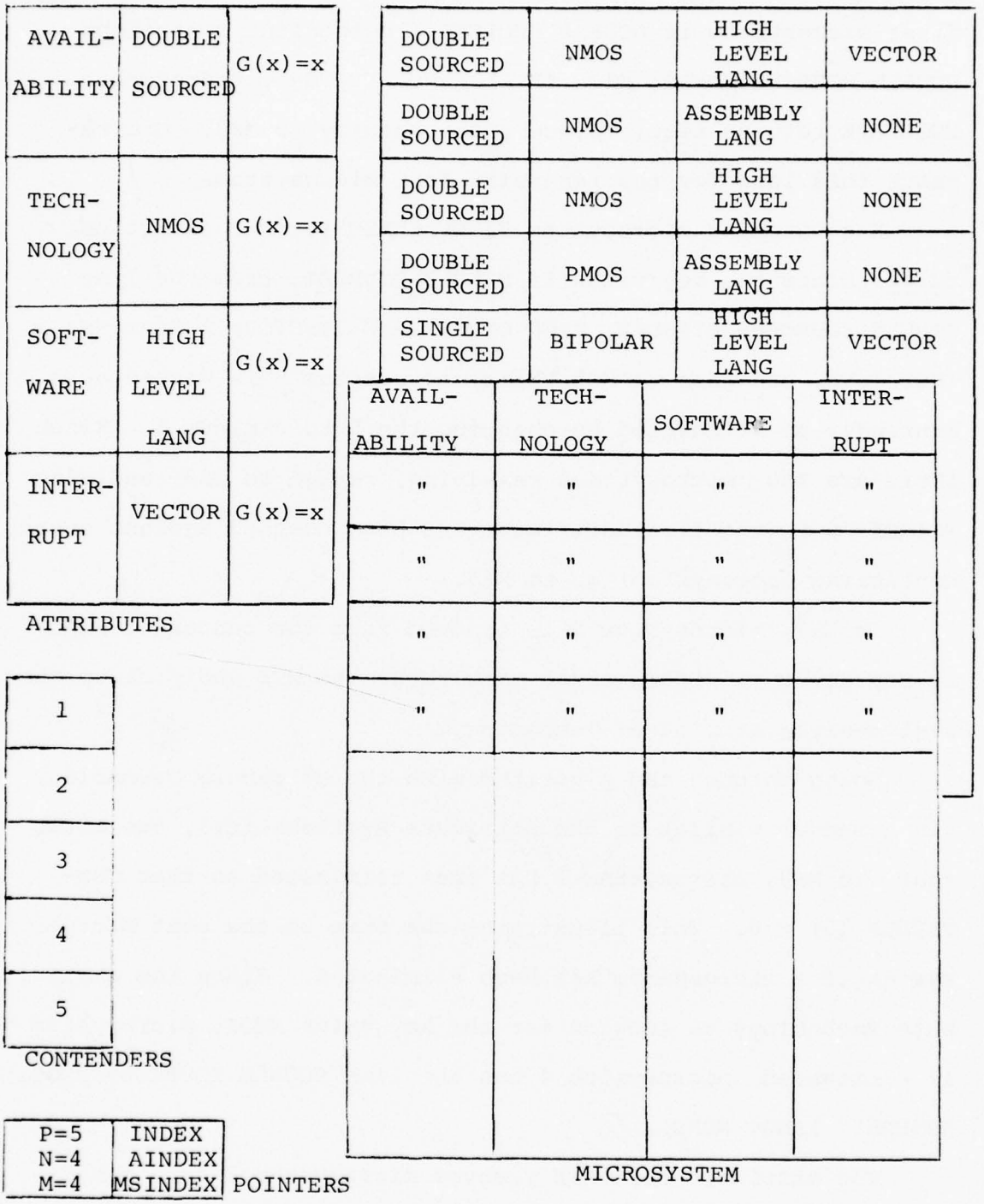


FIG. 7 EXAMPLE DATA INPUTS

first microsystem is DOUBLE SOURCED (in the line containing DOUBLE SOURCED, NMOS, HIGH LEVEL LANG, VECTOR), therefore EVALUATE returns true. Since true, returns to MS3. One repeats this loop for the remaining four microsystems.

Encountering microsystem 5, EVALUATE returns the value false (since the key value is SINGLE SOURCED, from the line SINGLE SOURCED, BIPOLAR, HIGH LEVEL LANG, VECTOR). From MS4, therefore, one goes to MS5 where microsystem 5 is marked as a contender to be deleted by changing the 5 to a minus 5. Since there are four microsystems remaining, return to MS3; and since MSINDEX > P (the first attribute has been checked against every contending microsystem) go to MS7.

In MS7, microsystem 5 is removed from the contender list by replacing -5 with a zero. Now return to MS2 and pick up the next desired attribute, Technology.

Going through the algorithm with the attribute Technology (in a manner similar to the attribute Availability), one notes that, in MS3, microsystem 5 has been eliminated so that CONTENDER (5) = 0. This illustrates the skip to the next microsystem if a microsystem has been eliminated. Since the attribute Technology is looking for the key value NMOS, microsystem 4 is eliminated (microsystem 4 has the line DOUBLE SOURCED, PMOS, ASSEMBLY LANG, NONE).

The attribute SOFTWARE removes microsystem 2 in a manner similar to that described above, and the attribute INTERRUPT removes microsystem 3. Thus, microsystem 1 is the selection.

3.3 RATIONALE BEHIND THE ATTRIBUTE STRUCTURE

3.3.1 Ordering by Hierarchical-Decomposition

The basic process used in developing the proposed selection algorithm could be called hierarchical-decomposition. The technique involves both analysis and synthesis, that is, both taking apart the subject under study and putting it together. The process of taking apart the subject is known more specifically as top-down analysis, and consists of successively imposing increasingly specific constraints, thus converging on an ultimate solution. The process of synthesis is known more specifically as bottom-up synthesis, and consists of successively combining blocks of lower-levels which have satisfied their individual constraints.

A mixture of analysis and synthesis is necessary because pure analysis becomes too difficult to modularize at low-levels, and pure synthesis becomes too complex to manipulate at higher levels. Combined in the proposed selection algorithm are the good high-level qualities of analysis and the low-level qualities of synthesis, joined to form a single procedure. The hierarchy proposed for the selection algorithm is presented in Figure 4.

Examining the attributes in order from top to bottom, it can be seen that top-down analysis is used to describe architectural aspects of microsystems; synthesis is used to compare low-level circuitry, such as the number of registers and their interconnection. Each attribute works on a succes-

sively more restricted subset of the original microsystem contenders as diagrammatically shown in Figure 8.

3.3.2 Justification of the Attributes

The attributes proposed by the algorithm are intuitively defended as necessary and sufficient by explaining what areas they cover, while other proposals are shown to be extraneous. Figure 9 outlines basic features influenced by each.

The application criterion. The application criterion was included first in order to establish some general class-criterion for the design which will be used for decision making in subsequent attributes. It is important to include this factor because the later attributes must be approached with an overview of the system in mind; least important features be overlooked early in the selection process, and become inaccessable later on. Thus, the application attribute acts as a plateau from which one can view and plan the remaining attributes. An example of the application criterion is a Data Acquisition and Control type microsystem which might require: wide word lengths, numeric computation ability, speed, ability to react in real time, interrupt capability, and the ability to easily interface to analog signal sources.

The availability criterion. This is included next because it is the most general area, and its five key values clearly, immutably, and specifically divide the microsystem products. (e.g. A microsystem is either available or not available,

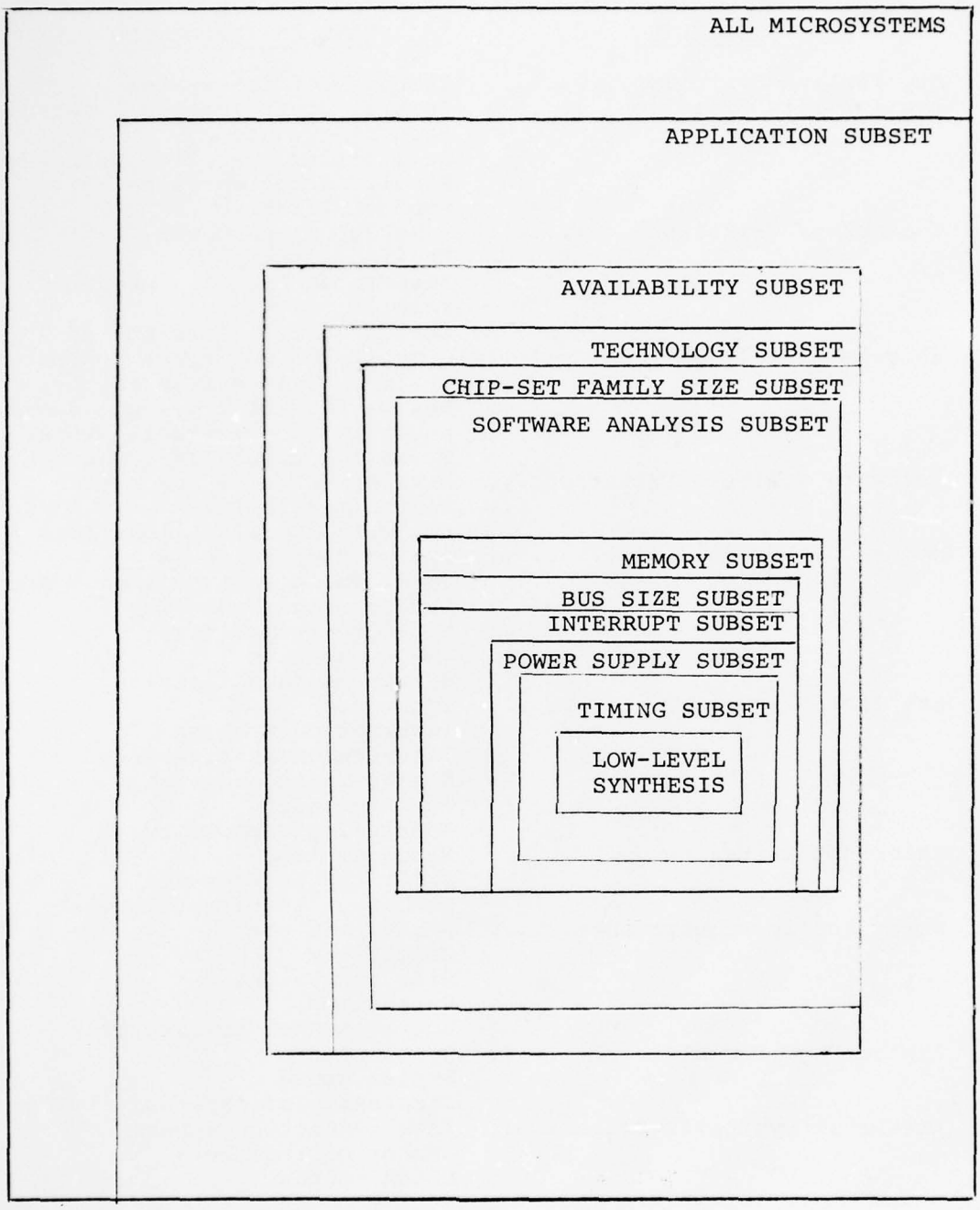


FIG. 8 TOP-DOWN ANALYSIS WORKS ON SUCCESSIVELY MORE RESTRICTED SUBSETS OF MICROSYSTEMS

ATTRIBUTE	FEATURES INFLUENCED
Application Criterion.....	Overview of the system
Availability Criterion.....	Initial costs (design & set-up)
	Recurring costs
	Reliability & serviceability
	Timely market entrance
	Product lifetime
Technology Criterion.....	Inherent speed-power
	Packing density
	Interface circuitry required
	Initial costs
	Environmental restrictions
Chip-Set Family Size Criterion.	Quantity of interface support
	Quality of interface support
	Design flexibility, expandable
	Built-in computational excess
	Evolution capability(longevity)
Software Analysis Criterion....	Development time and cost
	Design feasibility
	Hardware specifications (mem.)
Memory Requirements.....	Design support costs
	Development & production costs
	Programming complexity
	Microprogrammability
	DMA capability
	System expandability
Bus Size Criterion.....	I/O rates
	Instruction Cycling
	Instruction multiplexing
	Memory speed and size
	Package count
	Addressing capability
Interrupt Criterion.....	Response time
	Priority measurements
	Number of interrupt levels
Power Supply Requirements.....	Production costs
	Complexity
	Size and weight
	Durability
	Environmental restrictions
Timing Requirements.....	System costs
	System speed
	Complexity of external timing
Low-Level Synthesis Criterion..	Interconnection scheme
	Number of registers
	Stack depths

FIG. 9 BASIC FEATURES INFLUENCED BY EACH ATTRIBUTE

there is no grey area of indecision.) The five key values of the availability criterion may be found in Figure 4. It is important to include this factor because design costs, set-up costs, final costs, product reliability, serviceability, and product lifetime all depend on the availability of the components.

The technology criterion. This is included third because it directly influences the most critical areas of concern in discussing today's microsystems: speed, power requirements and packing density. It is additionally important to include this because interface circuitry, packaging, cost, and environmental requirements all also figure into the choice of a technology.

The chip-set family size criterion. This is given fourth priority in order to establish what kind and how much interfacing and support is to be provided with the chip; and how much will be done in-house. (e.g. Some applications require just a simple CPU to be surrounded by in-house circuitry, while other applications may require a chip-set family to function as an autonomomous unit.) It is important to include this factor because the chip-set family influences the quantity and quality of interface support; the architectural flexibility of the microsystem; the weight, size, and shape of the microsystem; the excess computational power paid for; and the longevity (evolutionary capability) of the final product.

The software analysis criterion. This was included fifth, and prior to the strictly hardware decisions, because it is recog-

nized that over 50% of the microsystem development time and cost will be software oriented. It is important to include this factor because development time and cost, design feasibility, and most hardware requirements all depend on the software available.

The memory requirement criterion. This is included directly following the software criterion to stress that these two areas are directly related and interdependent. (e.g. The memory size required to do a specific task may vary widely according to the power of the instruction sets of the different microsystems under consideration.) It is important to include this factor because design costs, production costs, system expandability, flexibility, and speed are all influenced by the memory choice.

The bus size criterion. This was included next because the controversy of today of what bus size to use has conveniently broken microsystems into 2 (bit slice), 4 (bit slice), 8, and 16-bit partitions. It is important to include this factor because the bus size influences the I/O rates, instruction cycling and multiplexing, package count, and the addressing capability of the microsystem.

The interrupt criterion. This is included next to describe how all the various components are to share the available resources of the system. It is important to include this attribute because the response times, priority measurements, and the number of response levels are all dependent on the interrupt

capabilities of the individual microsystem.

The power supply requirements. These are included next to help bring into focus the cost of supplying power, and the probable complexity demanded in the external power supply circuitry. It is important to include this factor because environmental factors, cost, and support circuitry complexity are all dependent on the power supply requirements.

The timing requirements. These are included as the last of the analysis attributes because they, like the power supply requirements, influence the complexity of the user supplied support circuitry. It is important to include this attribute because it directly relates to system cost, speed, and complexity of external timing circuitry.

The low-level synthesis criterion. This is included to better analyse the low-level circuit charateristics of the remaining microsystems. It is important to include this attribute because pure top-down analysis becomes too complex at this point to handle effectively, while synthesis and comparison begin to work to their best advantage at the level of registers, stack and transistors. Comparison at this level, on the limited set produced by all the previous attributes, allows one to pick the best architectual fit for a final design specification.

3.3.3 Explanations of Omissions

This section has been included to record reasons of omission for various attributes proposed by other authors. Those potential attributes which have been considered but

omitted are listed below*:

1) Familiarity is not included as an attribute because having used the microsystem previously, one should be aware of how it compares to those chosen by the MS Algorithm.

2) Cost is not included as an attribute because it is a quality which can be distributed over several other key values, and not a specific, singular feature.

3) Vendor reputation is not included as an attribute because is too variable to use as a structured feature. Such value judgements are left as qualifiers (or adjectives) to consult when assigning specific numerical values to the attributes.

* This author would gratefully appreciate receiving input on possible additional attributes.

CHAPTER 4

USING THE SELECTION ALGORITHM

4.1 WHERE SELECTION FITS INTO SYSTEM DESIGN

In choosing the proper microsystem, it should first be decided if a microsystem is required. The high allure of semiconductor microsystems, memory, and I/O is causing many digital designers to forget that a microsystem is only one possible solution to digital design problems. The following list, compiled by Lane [7], defines those steps required in system design:

A) Decide on product or problem.
   1) Clearly state the objectives of the proposed design.
   2) What features and customer benefits does it provide?
   3) Is there an adequate market for the product?
B) Perform a system analysis.
   1) Define performance requirements and system I/O.
   2) Establish price and projected volume.
   3) Estimate design schedule and resources available.
C) Check alternatives to a complete microprocessor system.
   1) Minicomputer mainframe or board.
   2) Microcomputer system, board, or modules.
   3) PLAs, ROM state machine, MSI controller.
   4) Custom LSI.
D) Select the microprocessor, if you have decided to use one.
   1) Transform system analysis into selection criteria.
   2) Study alternatives based on application.
   3) Narrow field by eliminating obvious mismatches.
   4) Analyze vendor specifications and microcomputer designs.
   5) Do several tentative designs, if necessary.
   6) Make selection.
E) Plan the system.
   1) Use data gathered during selection process.

2) Organize design team for hardware, software, mechanical/packaging functions.
3) Schedule hardware and software.
4) Plan a software development system.
5) Set cost, flexibility and expansion/growth limits.

F) Design the system.
1) Ensure constant focus on product objectives.
2) Ensure communication between hardware and software personnel.
3) Review costs, design progress and changes in objectives.
4) Provide for test programs.

As can be seen from Mr. Lane's list, special care must be taken to decide if a microsystem is the best solution to the design problem. In fact, the selection process should not be attempted until the problem definition, system analysis, and alternative investigation phases have been completed.

4.2 THE SELECTION PROCESS

Suppose it has been decided that microsystems can offer good advantages to the design system, now the proper microsystem must be selected. It is noted in Chapter 3 that the selection algorithm operates on specifically defined data, called attributes. In the sections below, the attributes to be operated on by the MS Algorithm are discussed in detail.

4.2.1 Application Criterion

The first attribute in the selection algorithm, the application criterion, may be stated:

Decide in what general application category the system

may be classified, and note the general structures of importance in that category.

This attribute may be broken down into the following key values:

1) Data Acquisition and Control
2) Data Communications
3) Human Interface Equipment
4) Computational
5) Other

These key values divide microsystems into those which monitor systems (Data Acquisition and Control); those which are involved in network switching (Data Communications); those which communicate with the public as in point-of-sale terminals (Human Interface Equipment); those which are involved in numeric computation operations (Computational); and those which fall into none of the other classes, but are more general (Other).

This attribute is important because it forces a closer look at the system design on a general scale; an action which allows generalities to become more apparent, such as the probable word length, cost, storage-size, language levels, and speed required. There is no specific breakdown that will work for all designs. Rather, the user should analyze his own design and determine its needs. If it falls under one of the

first four categories where microsystem elimination may occur, then a subset of contending microsystems will be passed to the next attribute. Otherwise, the complete microsystem contender list will be passed. A general guide is presented below which gives the typical attributes each key value should contain. This is presented to give the user a feel for what is required of him at this point in the MS Algorithm.

Data acquisition and control. For this application a microsystem should offer:

1) Wide word length
2) Numerical computation ability
3) High speed
4) Ability to react in real time
5) Interrupt capability
6) Ability to easily interface to analog signal sources

Data communications. For this application a microsystem should offer:

1) High-speed data handling
2) Good file search
3) Error-code generation
4) Error-code checking
5) Easy interfacing to serial data lines

Human interface equipment. A microsystem for human interface should offer:

1) Low cost
2) Small parts count
3) High reliability
4) BCD arithmetic capability
5) Low speed
6) Some user programmability
7) Small word length

Computation. A computational microsystem should offer:

1) Large word length
2) Numerical computation ability
3) Low cost
4) Good interfacing to mass storage
5) High speed
6) Higher-level languages

Other. For general areas of microsystems no such list can be compiled, but rather the MS Algorithm passes all contending microsystems through to the next attribute unchanged. The designer should have prepared his own list to act as a guide in later attribute stations. Kaye [6]

Figure 10 shows some typical microsystem applications

APPLICATIONS	CROSS REFERENCE to the key values:
Microcomputers	4
Distributed Computers	4
Automatic Typesetting	5
Inventory Control	1, 2, 3, 4
Point-of-Sale Terminals	3
Other Terminals	3
Telecommunications	2
Smart Instruments	1, 3
Machine Control	1
Adaptive Traffic-Control	1, 2
I/O Channels for Large Computers	1, 4
Medical Systems	2, 3
Radio Navigation Equipment	2
Optical Character Recognition (OCR)	1, 3
Automated Test	1
Automatic Time Clocks and Payroll Systems	3, 5
Automotive Controllers	1, 5
Avionics	2, 3, 5

1) Data Acquisition and Control
2) Data Communications
3) Human Interface Equipment
4) Computational
5) Other

FIG. 10 TYPICAL MICROSYSTEM APPLICATIONS: Ref. [13]

and where they fit in this scheme.

4.2.2 Availability Criterion

The availability criterion is the second attribute in the selection algorithm. It may be stated as follows:

> Decide when the microsystem must be available for manufacturing of the system, and the level of product support necessary.

This attribute may be broken down into the following key values:

1) Double Sourced
2) Single Sourced
3) Threshold
4) Planned
5) Future

These key values divide classes of microsystems into those which have been on the market long enough to be manufactured by companies in addition to the original makers (Double sourced); those which are on the market only through the original manufacturers (Single sourced); those which are scheduled to be placed on the market immediately (Threshold); those which are only announced, and must be designed and tested yet (Planned); and those which are only projections of possible future designs (Future). This step is important be-

cause it eliminates those microsystems which won't be available at that point in time required by the system manufacturing stage, and those which are not yet fully documented and supported. These key values are examined in more detail below:

Double sourced microsystems. These microsystems are those which are produced by more than one manufacturer. In general, these are the lowest cost, most easily obtainable, and the most fully documented systems available. They are also the systems most likely to be tested, testable, and subject to error-free operation. One additional advantage is that the manufacturers are very unlikely to drop the product line completely when it becomes obsolete after investing so much money promoting his products and gaining so many customers. Rather, in the future, downward compatable products will most likely be provided which will allow for upgrading a system without completely throwing away old software and hardware investments. A disadvantage of a double sourced microsystem may be that it is well along in its life cycle, and might be unable to compete with products using newer technologies.

Single sourced microsystems. Microsystems of this class are those which either have not been available long enough for alternate sources to have begun development work on reproducing the component, or else the component is not yet considered popular enough (or good enough) to justify the expense of double sourcing the original manufacturer. The advantages of such microsystems are that they are in the early part of their life cycle

and may offer a longer useful life than older products. Also, the fact that they are more likely to contain the newer technologies developed since the introduction of older products, and to have learned to avoid some of the earlier generation's mistakes. This means that they may offer speed, power, and capability advantages over these older products. The disadvantages include the facts that the product may fail to develop competitively and thus remain a highly priced item, or be dropped totally from the market; documentation is apt to be incomplete and contain errors; product support may be too young and experience too limited to provide necessary assistance; and new ideas employed by the product have not been given the time necessary to demonstrate their performance.

Threshold microsystems. Threshold microsystems are those which have just left the manufacturing stage and are new on the market. These microsystems have the same disadvantages as single sourced microsystems; and to a lesser degree, the same advantages. The major decision here must be to either trust the reputation of the manufacturer to deliver a fully supported component or to choose a more proven product.

Planned microsystems. These microsystems are less likely to be considered for designs, but are included so that these ideas may be catalogued and kept under surveilence in order to help predict future trends in the market.

Future. As with planned microsystems, this key value is not likely to be considered for present implementations; but flex-

ibility forecasting may be enhanced by keeping track of advances predicted and projected by the microsystem manufacturers.

In general, it can be stated that the component cost of a microsystem is proportional to the number of different companies manufacturing the product. Thus, the higher the availability, the lower the cost. These systems are also the most fully supported and the lowest risk choices. On the other hand, the IC market is a fast moving field which renders most designs obsolete within two years. Unfortunately, it usually takes a year or two to really build up production of a product using IC's, so future predictions must be accurately made and the design components must reflect anticipated technological change in such a way as to minimize the total parts cost over the life of the product rather than simply the parts cost at design conception time. Blakeslee [2] looks at the normal life cycle of an IC. He points out that "when the product is first introduced, the price is quite high because, of course, the volume is zero. The price at this point has little relation to the cost to produce the part but is more a matter of strategy. If the component performs better than anything else available, it is not unusual to ask a very high price for it until competition develops; there are always designers who need higher performance and will pay almost any price for it. A large-quantity order at this point may go for one-fifth of the catalog price.

If the circuit is unsuccessful, no volume develops, no competition develops, and it dies. A successful product,

however, soon is 'second sourced' by other manufacturers. It thus enters a phase where competition forces the price down to something related to the actual manufacturing cost. As volume increases, price decreases. This is partly due to increased volume and partly due to the 'learning curve'. The learning curve is simply a decrease in manufacturing cost as more experience is accumulated from actually shipping the product, as shown in Figure 11. There is a learning curve for each circuit and another on for the process in general. Thus, a process (like bipolar, P-channel MOS, or N-channel MOS) also has a learning curve like the one shown in Figure 11. In addition; there is another curve, known as the life cycle, which is important to know for understanding the price of IC products. As shown in Figure 12, the speed with which the price of an individual circuit falls is related to the degree of development of the process used to manufacture it. The rate of decrease in price is always greater for a new part or process than for an older, more mature one.

After about two years of steadily increasing volume and steadily decreasing prices, a point is reached (maturity) where another, clearly superior product becomes available. From this point on, the price stops falling, but the volume continues to increase for a couple more years. The volume grows mainly because of continuing shipments of products using the circuit. There is no need to lower the price further because nobody will use the part in new designs anyway, and those who have it

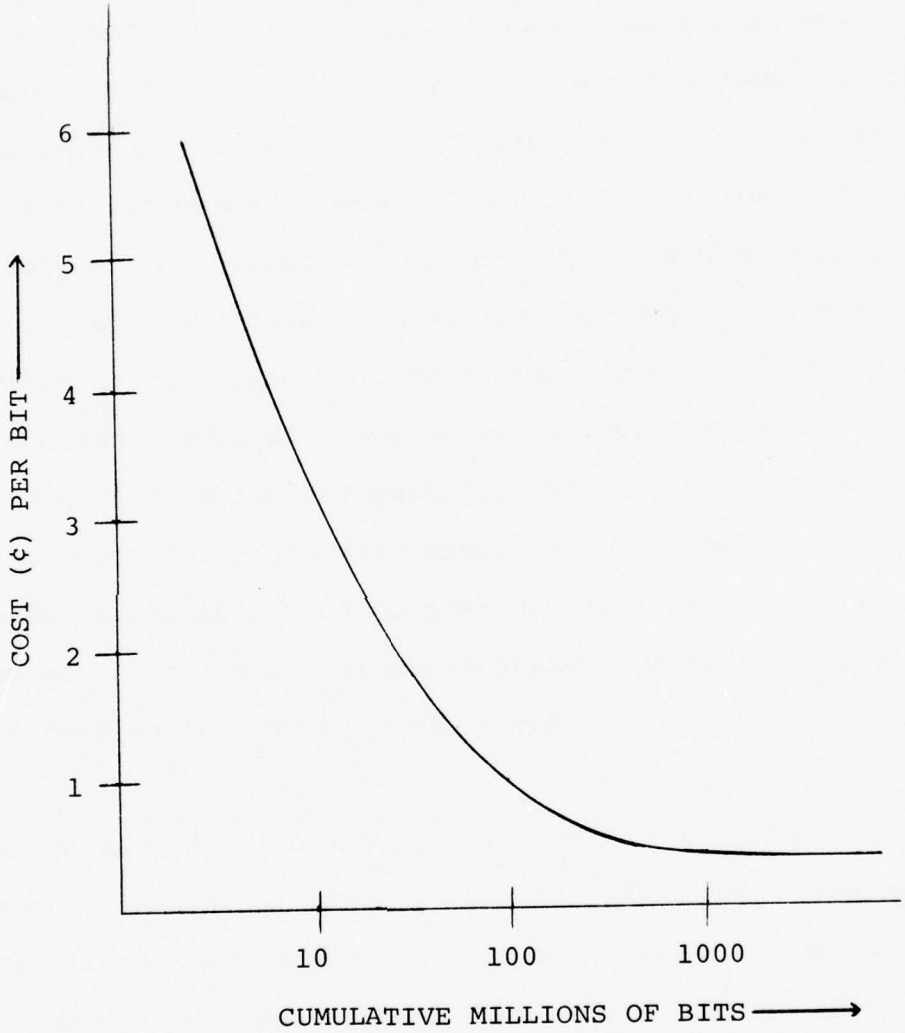


FIG. 11 TYPICAL PRICE-LEARNING CURVE: long shift register [2]

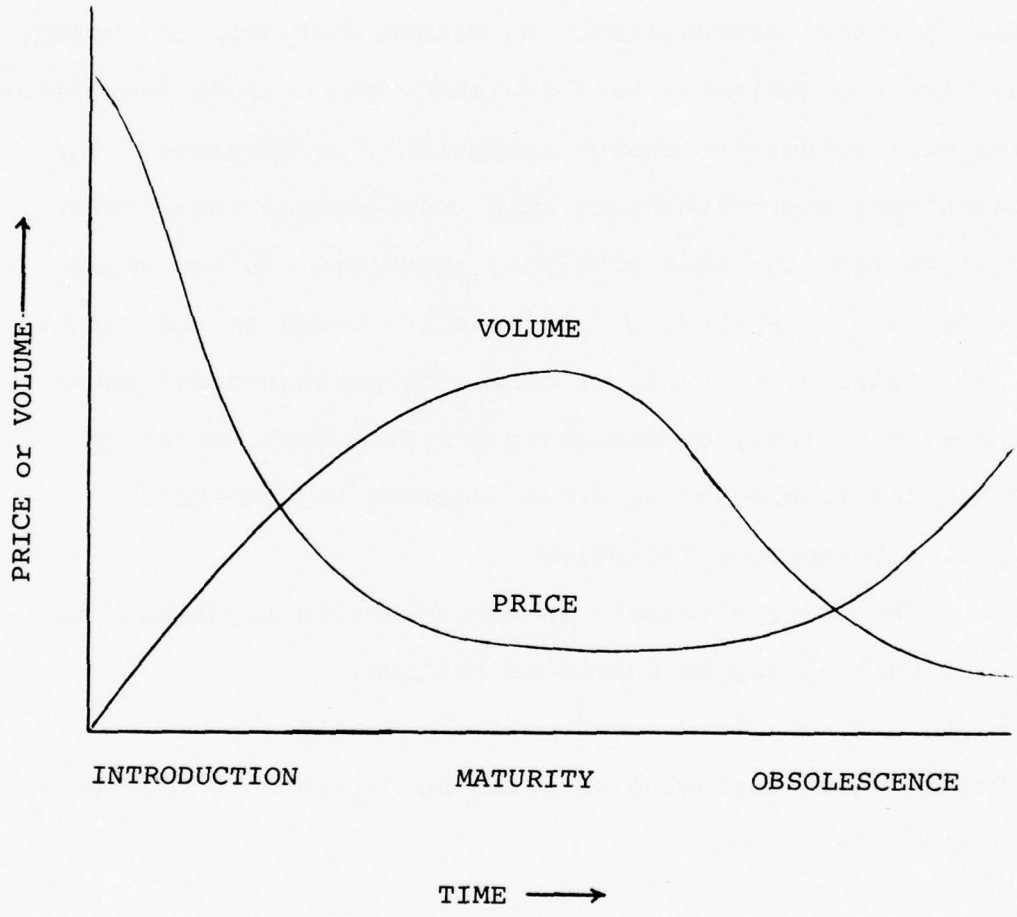


Fig. 12 IC PRODUCT LIFE CYCLE: Blakeslee [2]

designed in already are stuck with it. At this point the part is 'past its prime'. Finally, the part becomes obsolete; the volume starts to fall, and eventually prices actually rise a little as the volume falls and manufacturers drop out of the market."

It should be noted that the designer shouldn't wait for the 'perfect' microsystem. No matter what chip is chosen, by the time the design is half finished, one or more new microsystems will render the design suboptimum, or obsolete. The LSI technology expansion makes this obsolescence inevitable. Competitors face the same problems; therefore, do not change the selected microsystem, or postpone it, based on what might soon be available. If this is done, the product development will never end. Only by designing a system that can be upgraded in the future can this obsolescence be combated.

4.2.3 Technology Criterion

The third attribute in the selection algorithm, technology criterion, may be stated as follows:

Decide which technologies would be suitable in the system design.

This attribute may be broken down into the following key values:

1) PMOS
2) NMOS

3) CMOS

4) IIL

5) TTL

6) OTHER (SOS, etc.)

These key values divide microprocessors into technology classes now used by manufacturers. These classes are positive-channel metal-oxide-semiconductors (PMOS); negative-channel metal-oxide-semiconductors (NMOS); complementary metal-oxide-semiconductors (CMOS); integrated injection logic (IIL); transistor-transistor logic (TTL); and others, such as silicon-on-sapphire (SOS).

This attribute is important because speed, cost, power consumption, weight, size and interfacing with the rest of a system all hinge on the type of technology used to manufacture a particular microprocessor. A more detailed discussion of each of these key values is presented below.

PMOS. P-channel MOS normally "operates" in an off mode until switched on by a minimum value of gate voltage which causes a channel formation between the source and drain. This makes for low power consumption, but creates one disadvantage in the need for different power supply values for the gate and the drain. Also the surface inversion carrier mobility for this process is relatively low which results in degraded circuit speed. Being the first technology used in microsystem design Intel 4004, 1971 it is the cheapest to use and the best understood.

However, in general it offers none of the second and third generation advances.

NMOS. The silicon-gate N-channel MOS process introduced in memory chips in 1973 has about a dozen laws of physics favoring it over PMOS. It makes components smaller, faster, cooler and more amenable to working with standard power supply voltages. The heavily doped p-type substrate can result in a low voltage threshold enhancement-mode device that can operate from a single +5 volt power supply with complete TTL compatibility. Easier mask alignment during fabrication allows for gate overlap of the source and drain regions to be minimized and capacitance reduced. This results in increased circuit speed. Also, the process allows greater internal interconnection complexity resulting in approximately a fivefold increase in both chip density and circuit speed over P-channel MOS. However, increased fabrication complexity adds to the cost.

CMOS. Complementary MOS technology makes it possible to reduce power dissipation to very small (50nW) levels by using complementary P-channel and N-channel enhancement MOS devices on the same chip. The N-channel transistor is usually the driver device and the P-channel transistor performs as the load. Only one transistor is on in a quiescent logic state. This arrangement leads to an extremely low standby power and high-speed operation. Other features are high noise immunity, TTL compatibility, single-power-supply operation and relative insensitivity to temperature variation. The high performance of CMOS

is somewhat compromised by the process complexity involved in circuit fabrication. Also, CMOS demands electrical isolation to preserve N-channel and P-channel devices as separate entities. Therefore, source and drain regions are not shared and must be separately connected with metallization. The isolation requirement and extra connections result in additional expenditure of silicon chip area (real estate) which proves to be another disadvantage.

IIL. Integrated injection logic, is an improved version of an old technology, direct-coupled transistor logic. The size and low-power advantages of IIL come from the shrinking of DCTL into a single complementary transistor equivalent. The resistor in the DCTL gate is replaced by an active current source; the emitter-grounded output transistor pair by a single multi-collector transistor, and a pnp transistor is added to serve as the current injector source. Thus, the six transistors of the three-input DCTL gate are reduced to a single transistor pair in IIL. Because of these elements in common, the entire IIL gate can be configured on silicon in the area it normally takes to place a single multi-emitter transistor.

IIL structure can take on two forms: isolated and non-isolated. The more common isolated form makes use of a conventional reverse-bias pn junction for component isolation which completely separates adjacent devices, therefore its use in circuits containing mixed-component functions.

Isolated IIL allows all other standard bipolar and

MOS design techniques to be combined directly with the IIL gates. Microprocessors [1] reports that this will bring forth the age where along with IIL digital sections on chips will be placed such linear and special buffer functions as LED drivers, memory decoders, current regulators, op amps, comparitors, oscillators, and very fast TTL or ECL logic.

Non-isolated IIL is the form that allows the most dense and efficient bipolar logic yet devised. Using a single transistor switch with a common ground plate, IIL takes advantage of the high carrier mobility inherently found in the bulk silicon structure. These IIL gates are capable of operating at nanosecond speeds, microwatt power dissipations, and a component density ten times that of TTL and twice that of MOS techniques. All of this can be accomplished in only four mask steps, two diffusions, and at high yields. Thus, the advantages of IIL may be summed up as a simpler process complexity, smaller gate size, and speed-power advantage. Unlike CMOS, IIL gates can operate at speeds of 10 to 20 nseconds while maintaining a constant speed-power product.

TTL. Transistor-transistor logic is the fastest logic currently in use; but also has the highest power and heat dissipation. It has the advantage of adequate performance for most applications, its very low cost, its availability, the large number of well established support suppliers, and the familiarity most designers have with using it. Its disadvantages are high power dissipations, low component densities, and the process is very

complex. Figure 13 shows a comparison of TTL with IIL.

SOS. Silicon on sapphire was originally developed for applications in the military and aerospace fields, and is a high-performance technology. The sapphire constitutes a nearly perfect substrate. Its insulating properties reduce capacitances and charing currents. Leakage currents become negligible. Because of these properties, packing densities exceed those obtainable in bulk silicon technologies, and speed is three to five times greater. Typical propagation delays are 5 to 10 ns, depending on such factors as fanout, and can go as low as 2 ns. Furthermore, absence of leakage between gates means that less power is required than for N-channel or P-channel MOS. Since the devices are completely isolated, there is no capacitive coupling between devices. This results in an order of magnitude increase in circuit performance in comparison to conventional CMOS. Disadvantages of this method are the complexities of process and most importantly to the user, the cost.

In general, the major technologies are best summed up by the figures on the next few pages. As can be seen from these figures, Schottky TTL provides high-performance, multiple chip-set microsystems; MOS/LSI provides high function density and the low power amenable for single chip microsystems (or at least a smaller number of chips); with SOS, IIL, and other newer technologies proving to be a strong challenge to both these older technologies performance-wise. There is a speed-

PARAMETER	I^2L	TTL
PACKING DENSITY (7um MASK DETAILS)	120-200 gates/mm^2	20
SPEED POWER PRODUCT	4-.2 pJ/gate	100
GATE DELAY	25-250ns	10
POWER DISSIPATION	6nW-70uW	10mW
SUPPLY VOLTAGE	1-15V	3-73V
LOGIC VOLTAGE SWING	.6V	5V
CURRENT RANGE (PER GATE)	1nA-1mA	2mA

FIG. 13 COMPARING I^2L WITH TTL: Altman [1]

power tradeoff involved here, with several of the newer technologies bridging the gap. Figure 14 shows how the various technologies compare according to their speeds, and where they find their most advantageous application. Figure 15 shows graphically the speed-power relationships among the technologies and Figure 16 the size (real estate usage) relationship. Using a more general component density scale, Figure 17 compares bipolar products (such as TTL, I^2L) against MOS.

Choosing for the future cost. As in the availability criterion, a technology must be chosen with an eye on the positional aspects of its life-cycle. Figures 18 and 19 show how the prices for technology change on a yearly basis, and the performance improvements that accompany them.

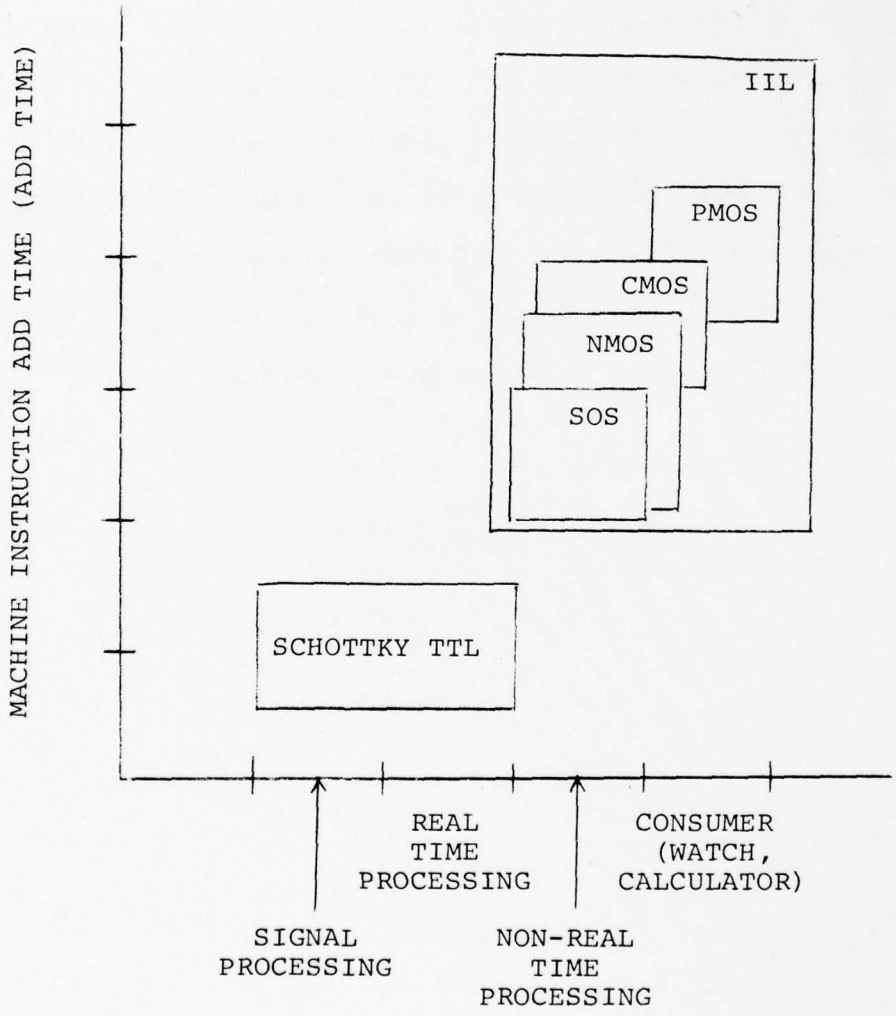


FIG. 14 USE AND SPEED LIMITATIONS OF TECHNOLOGIES: Ref. [1,13]

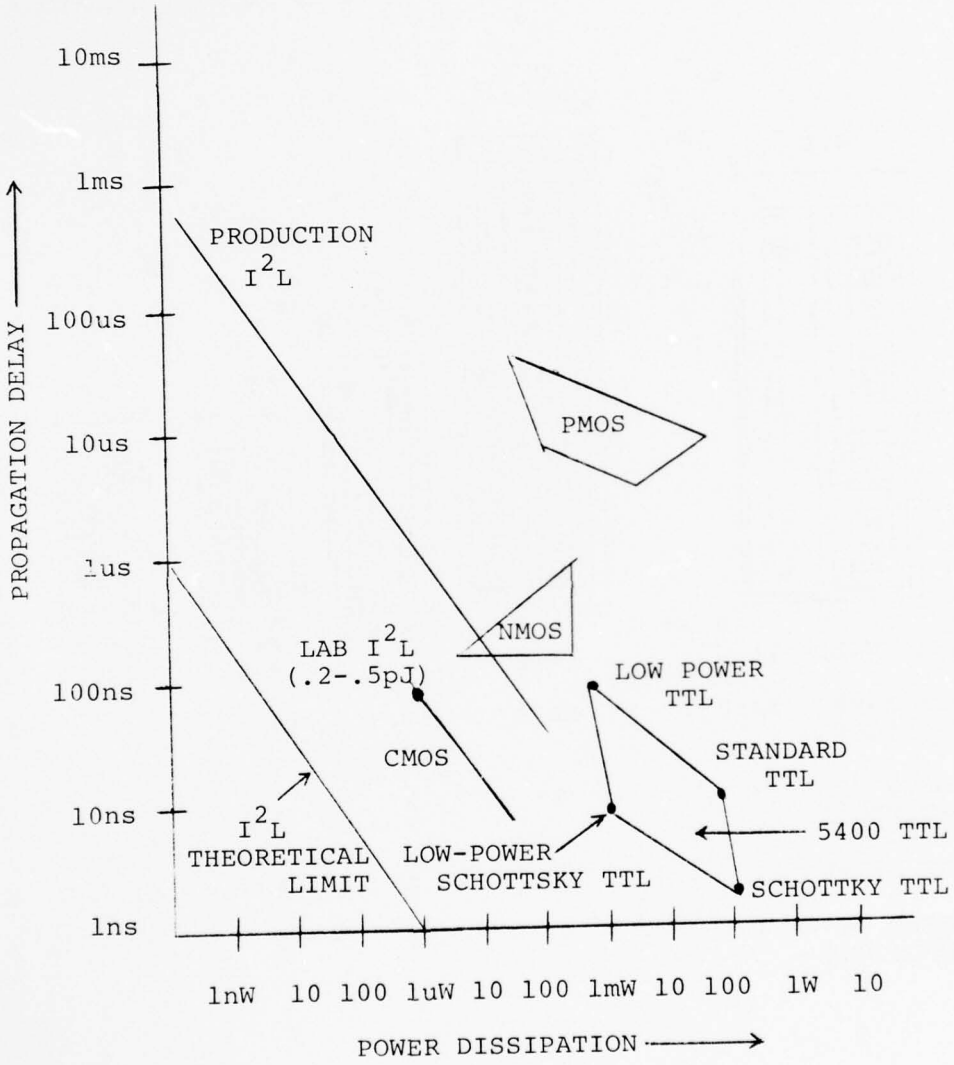
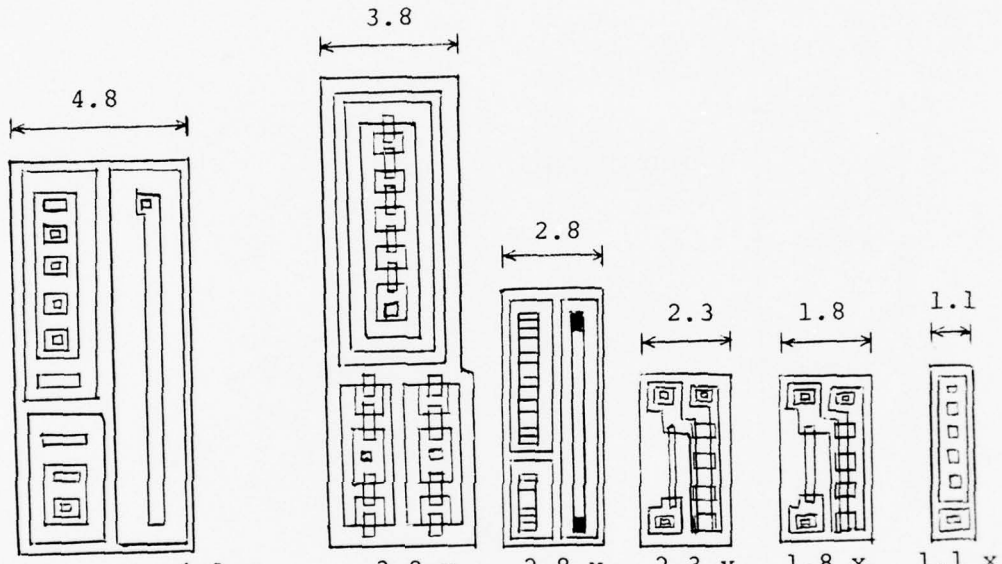


FIG. 15 SPEED-POWER OF THE TECHNOLOGIES: Ref. [1,13]

(ALL STRUCTURES 4-WIDE GATES, ALL DIMENSIONS IN MILS)



	STD TTL MSI	C-MOS	TTL LSI	P-MOS	SG-NMOS	I^2L
SIZE (MIL)	4.8 x 11.0	3.8 x 13.1	2.8 x 7.1	2.3 x 4.6	1.8 x 3.1	1.1 x 4.33
GATE AREA (SQ MILS)	52.8	49.8	19.9	10.6	5.6	4.8
NUMBER OF COMPONENTS	3	3	3	2	2	1
MASK STEPS	7	6	7	4	7	4
NUMBER OF DIFFUSIONS	4	3	4	1	3	2

FIG. 16 COMPARING THE SIZE OF TECHNOLOGY: Ref. [1,13]

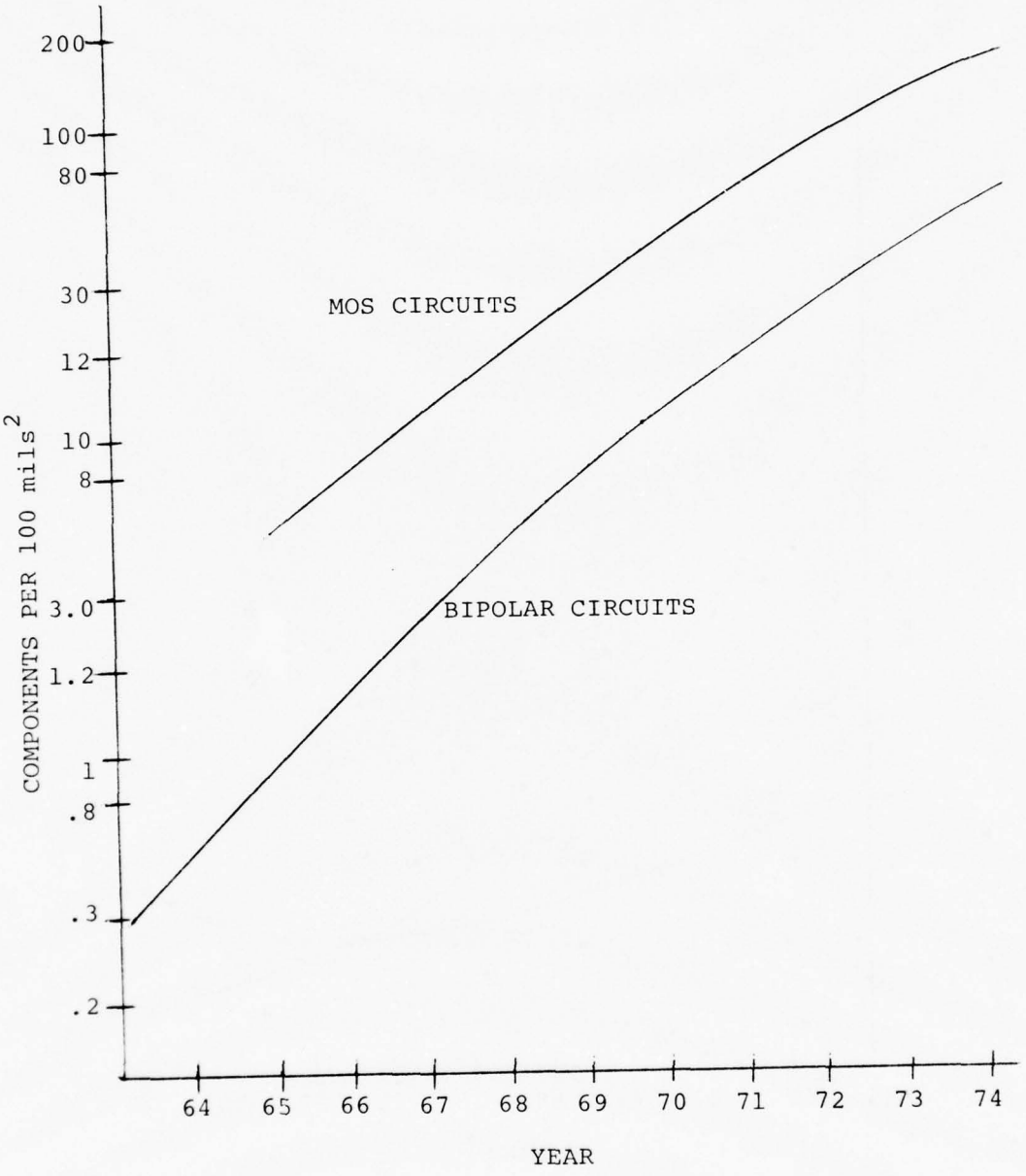


FIG. 17 COMPONENT DENSITY: Blakeslee [2]

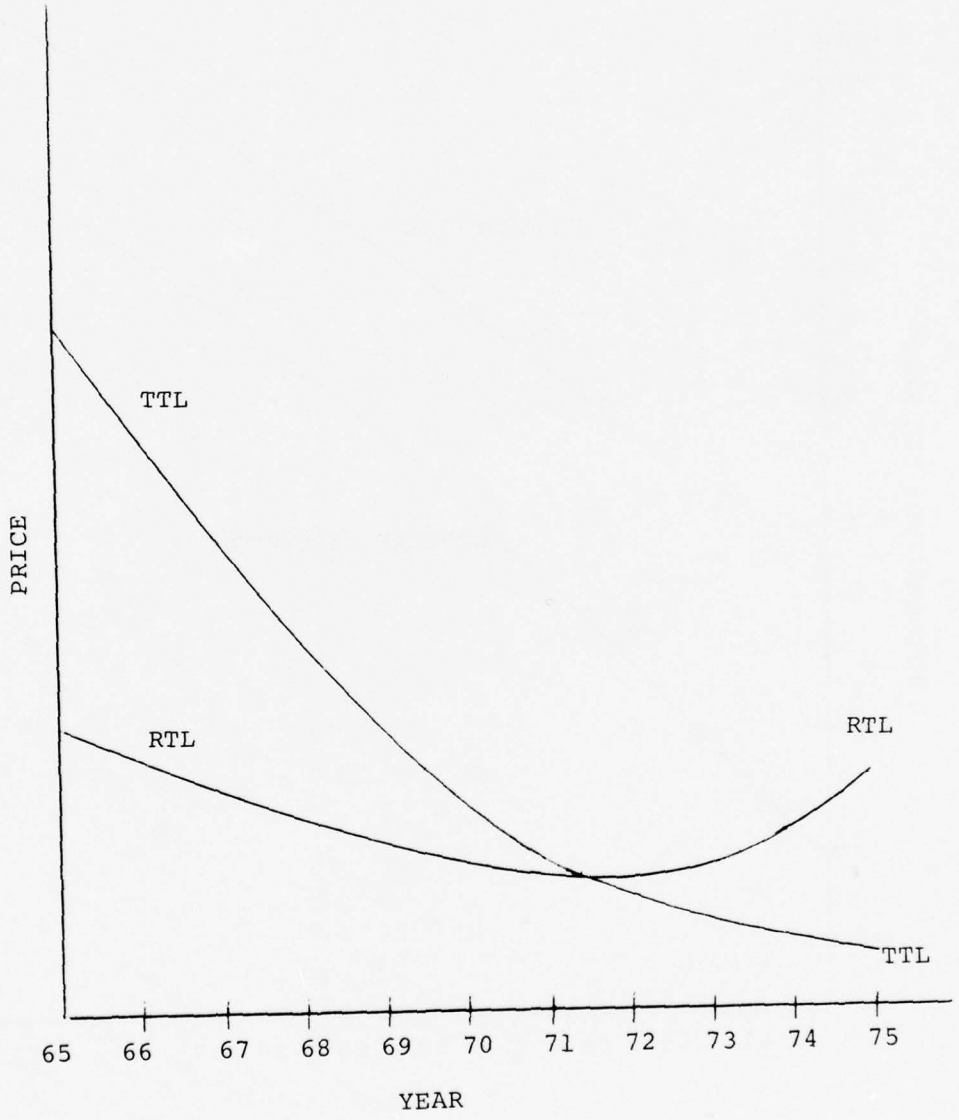


FIG. 18 SAMPLE FOR CHOOSING COMPONENTS FOR FUTURE COST (PRICES OF RTL & TTL GATES): Blakeslee [2]

MICROPROCESSOR FABRICATION PROCESSES

	TECHNOLOGY	CYCLE TIME (usec)	SPEED POWER PRODUCT (pJ)	PACKING DENSITY ($gates/mm^2$)
1972	PMOS	20	40	30
1973	NMOS	2	10	100
1974	TTL	.2	100	10
1975	IIL	.2	.5	100

FIG. 19 CIRCUITRY CAPABILITY IMPROVEMENTS: McPhillips [8]

4.2.4 Chip-Set Family Size

Chip-set family size is the fourth attribute in the selection algorithm. It may be stated as follows:

> Decide what types of chip-set families would be suitable in the system design.

This attribute may be broken down into the following key values:

1) Single Chip CPU
2) Bit Slice
3) Divided-Function Chip-Set
4) Single Board Computer (Kits)
5) Single Chip Computer

These key values divide microsystems into classes according to their architectural arrangement. Specifically these are: those microsystems providing a simple, yet complete, controller and memory on one chip to form a Single Chip CPU; those dividing the working bit length into some convenient manner which allows for expanding to any word size by simple interconnection of identical chips; those dividing the I/O, control, and memory into separate (but combinable) chips to form a Divided-Function Chip-Set; those providing a complete microsystem on one board; and, lastly, an area to contain future possibilities such as a universal logic module which could act as a single building

block, or single chip, with which any particular architecture could be built.

This step is important because it forces early decisions concerning the size, configuration and flexibility required of the selected microsystem in the overall system design. A more detailed discussion of each of these key values is presented below:

Single chip CPU. These microsystems were the first microsystems out on the market and are the least expensive microsystems available. With this advantage of cost, however, comes complexity in their use. Each microsystem in this area is vastly different from any other competitor's and requires the user to reorient his training and design around that microsystem. Also, these systems suffer from lack of regular support chips in their families. What results is that the user must design his system around the microsystem, not simply integrate it into a present system.

Bit slice. The bit slice architecture is an approach which offers the advantage of flexible word length. All chip functions are created to work on some base bit size which may be readily expanded by a simple interconnection of chips. This important variation to the fixed word length microsystem design uses either 2 bit or 4 bit 'slices' which can be used to create 8-, 12-, 16-, 24-, and 32-bit wide architectures. The longer word length for both addressing and instructions provides higher throughput and easier programming while the shorter

4-bit word length uses less hardware and smaller memories. This modular approach is used to build up the registers, arithmetic logic unit (ALU) and I/O data lines to 32-bit widths. This concept has been used for some time but software support and I/O interfaces for all models has not been practical in the past.

Divided-function chip-sets. These microsystems are those which incorporate on one chip those characteristics which work closely together. Separate chips are so designed as to be easily interconnected to form the final desired architecture. This type of arrangement offers many advantages, including maximum flexibility, low cost chips available due to increased yields (because a larger number of smaller chips may be formed from a single wafer of silicon), and it is possible to choose which functions are desirable for the design, without being forced to buy extraneous functions. Also, chip-sets are generally constructed with "ease-of-interfacing" in mind so that there is generally more pin-connection room, and standardizatio[illegible]han in other types of sets.

Single board computer (kits). Many manufacturers are now going to a single board approach which, in effect, gives the user a predesigned microcomputer he may simple plug into his system. Such a system consists of a central-processing unit, read/write and read-only memories, and parallel and serial input/output-interface components all placed together on one board. Three advantages can be observed from this arrangement. First, the

primary reason for the use of a single assembly of LSI devices rather than a multiboard system is economic. Extra board assemblies are costly in themselves and need related equipment, such as backplates and housings, that also add to the cost. Secondly, compactness and low power consumption are often required in products. Using LSI for all key computer functions possible reduces power consumption and allows a higher functional density than conventional subsystem assemblies. Lastly, a board containing all generally needed computing functions could be used as a standard part and thus take advantage of high product rates to lower its cost as far as possible, keep inventories simplier, and help standardize certain aspects of system design.

The same general idea is also available as a kit which must be assembled before use. Such kits are very useful for very small production because their cost is lower than preassembled boards and the hands-on experience gained in their construction is invaluable, but very rapidly the cost of their construction eats up any savings to be obtained from kit purchasing. In general, kits are useful only to the experimenter or hobbiest.

Single chip computers. The single chip computers of today are very simple machines and very limited in function. As its title says, it is a complete computer on a single chip. This offers the advantage of a small chip count (and thus lower overall system cost), fewer interconnection problems, and

freedom to look at the whole microsystem as a simple blackbox. However, this approach suffers from inflexibility, higher single chip costs due to size, complexity of manufacturing, and smaller yields. It also forces the user to accept all the internal functions of the chip (and pay for them) even if his design does not make use of them.

The chip-set size criterion describes the complexity of each microsystem, its ease of use, and the flexibility in design afforded by it. It is possible to obtain anything in the range from an isolated, simple CPU (controller chip) which operates as, and must be treated as, a discrete component; to a microcomputer board fully operational except for the teletype. For automotive-type applications, for example, it may only be necessary to have a small monitor do a few simple calculations every second and report any detrimental changes; for this a very low cost, simple CPU chip may fit perfectly into the design. At the other extreme, it may be desirable to have a OEM microcomputer board which may be simply plugged in and used immediately for intelligent terminal type operations.

Smaller families may become obsolete and be phased out of a company's product line, while larger families have a tendency to evolve into new technology with the introduction of down-ward compatable microsystems by microsystem manufacturers, making use of older developments possible.

4.2.5 Software Analysis Criterion

The fifth attribute in the selection algorithm is the software analysis criterion and may be stated as follows:

> Decide on the data structures required in the design and any special intructions; and note the requirements, or restrictions thus imposed.

Before describing the key values, it will be helpful to study a portion of an article by Theis [14]:

"In microprocessor applications the designer-programmer is trying to implement a design (previously done by logic designers on paper) through on-line programming of the microprocessor. Instead of using gate logic such as AND, OR, NAND and NOR, the designer-programmer uses the mask, compare, and jump instructions. Most microprocessor applications involve a mixture of control operations and application computations which are interleaved in the program mainstream. Assembly language is predominant. Because of modularity and the obvious repetitious nature of so many operations, subroutines are used extensively, and subroutine nesting is facilitated by the stack register organizations in all these units.

Software development for microcomputers is done several ways:

1) A designer-programmer may spend lots of time using paper tape to assemble with the microcomputer itself. In addition to the assembler, loaders for the assembled programs

and diagnostics to check out the hardware are available to him. Though not always offered, a monitor or executive rather than a full-blown operating system is sufficient for microcomputers since the machines are used in dedicated applications, not for general-purpose programming.

2) The designer-programmer may instead use a large-scale host computer (e.g. IBM 370) available through a time-sharing service to access an assembler which is usually written in FORTRAN (such program products are usually referred to as cross assemblers). An instruction simulator (also written in FORTRAN) executes the cross assembler output code as if it were being executed in the microcomputer. Higher level languages (e.g. Intel's PL/M) are also available to save the programmer time, but do not relieve him from debugging and checking out the compiled code, an operation which requires an understanding at the machine operation level.

3) A third approach uses a combination of hardware and software called a prototyping system. Prototyping systems provide program assembly, on-line execution and debugging. A general purpose prototyping system allows the designer-programmer to be more creative and productive in the design of a particular microcomputer application. As a result companies in this business either design a prototyping system as their first product or buy it. Using an on-line teleprinter, the designer-programmer assembles, edits, and stores the program in RAM associated with a computer in the prototype system.

Switching to the 'operate' mode the microprocessor in the application system accesses the program in the prototyping system as if it were in its own ROM and check out begins."

This attribute may be broken down into the following key values:

1) Resident Assembler
2) Cross Assembler
3) Monitor
4) High Level Language
5) Instruction Simulator
6) Prototyping System
7) Special Instructions

These key values divide the area of software into levels of complexity. (That is, the more software design support modules chosen by the user, the simpler his software production tasks.) The most complex software development task is taken when just a resident assembler is chosen; the tasks become easier as a cross assembler is used; and so on through to the prototyping system support selection. Each of these key values is discussed in more detail below:

Resident assemblers. The most complicated software development method to use, yet the least expensive, are resident assemblers. Using this system involves learning a specific assembly lan-

guage, programming in assembly language, and spending time condensing programs to fit the size restrictions of the resident space. Debugging, a major portion of the software development, is an extremely long and arduous procedure.

Cross assemblers. A cross assembler translates a symbolic representation of instructions and data into a form which can be loaded and executed later on by the microsystem. By cross assembler, what is meant is an assembler executing on a machine other than the microsystem, which generates code usable by the microsystem. Initial development time can be significantly reduced by taking advantage of the facilities of a large scale computer system such as its processing, editing capabilities, high speed peripheral capability, and the previous experience acquired by running the larger machines. An obvious disadvantage to this scheme is that a small organization may not have the larger computer to use, or cannot afford to rent one.

Monitor. The monitor is a simplified OS, or a master control program that observes, supervises, controls, or verifies the operations of the system. When a machine is being simulated on itself, one has the special case of a simulator with this simulator being considered the monitor, or trace routine. Such programs are used to help in the debugging of user programs since they print out step-by-step accounts of how the simulated program behaves. A typical system monitor loads and punches paper tape, displays and alters the contents of memory, fills memory with constants, executes programs in memory, moves

blocks of data in memory, and programs PROMs.

When the system includes a monitor, resident assembler, and an editor, the programmer can prepare his program in mnemonic form, load it into the microsystem, edit and modify it, then assemble it and use the monitor to load the assembled program.

High level language. Tests performed by Intel [3] on sample programs for microsystems indicate a high level language may be written in less than 10% of the time it takes to write the program in assembly language, and without much efficiency loss. The savings in time is related to the fact that the programmer can define his problem in terms more familiar to him, rather than terms more familiar to the computer. Debug and checkout time is also said to be much less than that of assembly language programs because writing in a high level language encourages good programming techniques. Presented below is part of an Intel report [3] on their own high level language, PL/M:

> "PL/M vs ASSEMBLY LANGUAGE
> As an example of comparative programming effort between PL/M and assembly language, a program to compute prime numbers was written twice, first in PL/M, and then in assembly language. The PL/M version was written in fifteen minutes, compiled correctly on the second try (an 'end' was omitted the first time) and ran correctly the first time. The program was then coded in Intel MCS-8 assembly language. Coding took four hours, program entry and editing another two hours, debug took an hour to find incorrect register designation, the kind of problem completely eliminated by coding in PL/M. Results of this one short test shows a 28 to 1 reduction in coding time.

This ratio may be somewhat high, overall ratio in a mix of programs is more on the order of 10 to 1."

The PL/M program took 15 lines to encode, the assembly language program approached 100 lines.

Instruction simulator. A simulator is a computer language written in some high level language which provides software simulation of the microsystem, along with execution commands from peripheral devices such as a terminal, card reader or disk file. These execution commands allow manipulation of the simulated memory and registers. An excellent feature is that operand and instruction breakpoints may be set up to stop execution at critical points in the program to allow closer study. Tracing features may also be provided which allow for monitoring of the CPU. As in the cross assembler scheme, access to a larger computer is a requirement of this approach which may prove inhibitive to smaller users.

Prototyping. As Mr. Theis stated, prototyping systems use a combination of hardware and software to provide general purpose simulation of program assembly, on-line execution, and debugging. A prototyping system is most useful for those users who will be designing multiple systems, and don't want to pay for a specific simulator for each individual design. A prototyping system for just one task may prove to be more expensive than a simpler simulator.

Special instructions. For many tasks, a particular instruction (or set of instruction types) in the microsystem's instruction

set may provide a particularly important operation to be requested by a single command rather than a program sequence. In fact, some special instructions may not even be emulated by a program sequence on some microsystems. In this case, one must either do without the special instruction, or else eliminate all those which can't handle it.

Software is the most expensive part of most systems today, and much effort is currently being made to understand the complexities involved in developing and maintaining it. The most commonly used method of comparing the software aspects of microsystems is to use benchmark programs. These benchmark programs are simply the implementation of a basic programmed function on each microsystem under test and then evaluating each microsystem according to its performance in completing the assigned task. However, to completely analyze and compare the software of microsystems is, today, a monumental problem. In general, it seems that the easier it is for the programmer to converse in his own natural language, the faster and better he performs.

4.2.6 Memory Requirements

The memory requirements attribute may be stated in the following terms:

> Decide the types of memory required (RAM, ROM, PROM), approximately how much of each type is necessary for the design, and how they are to perform.

This attribute may be broken down into the following key values:

1) Type/Size
2) Microprogrammable
3) DMA
4) Asynchronous Operation

These key values are discussed in more detail:

Memory section. The memory section of a microsystem usually accounts for a major portion of the chips. All three kinds of memory are used in microsystems. Random access memory (RAM) chips are used primarily for variable data and scratch pad. Read-Only Memory (ROM) chips are used to store instruction sequences. Programmable Read-Only Memory (PROM) chips are used for quickly tailoring the general purpose microsystems for specific applications. Because of the bus and word-size limitations of the microprocessor, it is not advisable to choose a system with more than 64K word memory. However, the amount of memory allotted should be based on a very conservative estimate of needs, because software costs go out of sight as the computer approaches 100% memory utilization.

RAMs are expensive compared to ROMs, but the data in the ROMs must be stored at the time they are created, so there is a production delay associated with them as well as a "programming" cost for mask development. PROM chips, some of

which can be erased by ultraviolet light and reprogrammed, are used in place of ROMs when small quantities are involved, because of their reusability property. This is not yet cost-justified for large runs.

Pin limitations off-chip to memory result in memory I/O times being fairly high; therefore, most architectures use an on-chip pushdown stack of some sort rather than requiring all storage to be contained in memory. Thus, the stack helps the programmer minimize register transfers, facilitates counting and sorting, and limits needless transfers to and from main memory.

Microprogrammability. The technique of microprogramming has also proven to be a very practical approach for microprocessor design. The primary advantages of putting the instruction set in control store are low cost, open-ended design and high utilization of LSI standardized products. These advantages are not without some disadvantages, however. When new instructions or functions are put in the microcode, the original designer has to change the support software, such as cross assemblers. The advantage of a microprogrammable architecture is therefore limited if the instruction set is to be significantly modified. Thus, a microprogrammable processor is one in which the instruction set is not firmly fixed. The instruction set is stored in a memory, the contents of which are fetched and used to control the internal data paths of the system. (Because the instruction is stored in a memory, it may be

MEMORY	SHAPE	ACCESS TIME (usec)	TECHNOLOGY	CENT/BIT (@ 100)
RAM	1024 x 1	1.	NMOS	1.5
	256 x 4	0.8	NMOS	1.6
	4096 x 1	1.*	NMOS	.4
	256 x 1	0.07	SCHOTTKY	5.1
ROM	2048 x 8	1.2	NMOS	.2
	256 x 8	1.	PMOS	1.2
	1024 x 8	0.45	NMOS	1.8
	512 x 8	0.07	SCHOTTKY	3.0
PROM	256 x 8	1.	NMOS**	1.5
	512 x 8	0.5	NMOS**	2.4
	512 x 8	0.1	SCHOTTKY	3.8
	256 x 4	0.07	SCHOTTKY	2.0

Notes: *Dynamic
**Erasable PROM

FIG. 20 A SUMMARY OF FEATURES AND COSTS FOR POPULAR MICRO-PROCESSOR MEMORY COMPONENTS: Ogdin [11]

changed as easily as changing any data value in memory.)

DMA. With direct memory access (DMA), waiting delays for memory access time are reduced by providing separate registers for the addresses, and sufficient extra logic and data paths to allow all aspects of actual data transfer to take place completely independent of the central processing unit (CPU). In this way, whenever the CPU is not actually accessing memory, the I/O channel can "steal a memory cycle" from the CPU. (Another popular name for DMA is cycle stealing access.)

Asynchronous. Memory organizations capable of asynchronous operations can significantly affect the performance and flexibility. This control function allows a microsystem to wait for memory or I/O. A small system, in which all components are access-time compatible, may not require this asynchronous memory access, but as soon as one mixes memory types and speeds (including refreshing of dynamic 4K types), the need for an asynchronous memory capability becomes crucial.

4.2.7 Bus Size Criterion

The seventh attribute in the selection algorithm, bus size criterion may be stated as follows:

> Decide on the bus bit-width requirement of the system based on the information of the previous attributes. These buses may include internal connective buses and external connectors, data buses, address buses, and instruction word buses.

This attribute may be more completely specified by defining the following key values:

1) Four-Bits
2) Eight-Bits
3) Sixteen-Bits
4) Other Sizes (12-, 32-bits)

These key values conveniently break microsystems into classes imposed by the industry. Most specialists agree the word length can be optimized for some applications, but that most word lengths will work for almost any application. The advantages and disadvantages of the four different classes are discussed in more detail:

Four-bit. If the application is BCD arithmetic, 4-bit microsystems are ideal. If, however, high precision, or communication with wide-word systems elsewhere in the system is required, four-bit microsystems prove to be too slow to compete with the larger word width systems. This is because larger width instructions or data words must be broken down into components of 4-bit widths and transmitted one component at a time. This size microsystem does, however, enjoy a comparitive simplicity and cost advantage over larger systems if speed is of limited importance.

Eight-bit. The eight-bit microsystems are the most commonly used systems, especially in controllers. They presently offer

the best performance as general purpose type machines. To a lesser degree, they suffer from speed bottlenecks in processing large word widths just as do the four-bit machines. However, they work well with byte size information.

Although the 8-bit microsystems now dominate the market, the introduction of 16-bit microsystems has prompted many 8-bit microsystems manufacturers to provide new enhanced 8-bit processors. Although 16-bit manufacturers refer to these enhanced machines as only stop-gap measures, the enhanced model manufacturers believe that the 8-bit microsystems are better suited to the low-end of the processor market; and, according to Wolff [16], should capture 35% of the dollars and even a higher percentage of units sold (compared to 6% of total dollars for the high-end 16-bit machines). The general impression is that 8-bit machines offer the performance required for most jobs, at a price lower than the 16-bit machines can now provide.

Sixteen-bit. The newest innovation on the market place is the sixteen-bit devices. With the introduction of these devices a big controversy is presently brewing over predictions that they will soon be edging the smaller width microsystems out of the market. Presently the cost is too high for them to be truely competitive with the 8-bit machines, but their makers predict that the cost will soon be equalized. Advantages offered by the sixteen-bit machines are quite clear in many applications. The foremost reason is the speed with which the newest processor generation can now execute a program. Since

eight-bit machines handle 16-bit data words and instructions by multiplexing in two cycling operations, the sixteen-bit machines halve this time. This advantage also simplifies the circuitry surrounding the microprocessor chip as well as the programs that must control the internal shuffling of data between registers.

Other sizes. The other size buses have offered no real benefits over the four-, eight-, or sixteen-bit microsystems. They are harder to use and to support. These are characteristically built of slice architectures and find their primary use in applications that demand bus sizes other than the standard ones.

In general, the biggest push in the industry now is between the eight-bit and sixteen-bit machines. This should be an influencing factor in lowering the costs of these sizes to their lowest levels. Other size buses seem to be doomed to repressed demand and maintain their higher than optimum cost. These 'odd' size buses do, however, offer a noticeable cost benefit in some applications because they more closely conform to the requirements without providing excess computational power.

The bus size and complexity depends on the type and size of the application, and the requirements concerning flexibility and expandability. Smaller systems can take advantage of recent trends in microsystem family components which allow the system bus to be nothing more than the bus offered on the

chip, while larger systems must be equipped with buffer elements or additional decoding logic to connect more functions to the system bus. Thus, one must be careful when choosing a bus structure that upgrading performance, flexibility, and expandability are not impaired. It is also important not to narrow the choice of acceptable memory and I/O devices since processor and memory speed can become the most valuable feature in a systems product life.

4.2.8 Interrupt Capability Requirements

The interrupt capability requirements attribute in the selection algorithm may be stated:

> Decide on the importance and probability of interrupts in the system, especially in regards to speed and nesting requirements.

This attribute may be broken down into the following key values:

1) Single-Line Interrupt
2) Multilevel Interrupt
3) Vectored Interrupt
4) No Interrupt

These key values divide microsystems into classes dependent on their type (and speed) of response to the situation where the CPU is interrupted to do something special before continuing

with its next instruction.

This attribute is important because it recognizes the fact that certain applications, or situations, may require CPU recognition instantly (least some irreversable action occur), while in other applications nothing disastrous occurs by delaying an interrupt request. The nature of most applications is such that if there is any chance at all of having to service any interrupt immediately, the CPU must be able to respond immediately. A more detailed look at each of the listed key values is presented next:

Single-line interrupt. The single-line (or single-level) interrupt capability provides a single interrupt line. Multiple interrupting devices must be OR-tied to that one line. When any interrupting device wants service, it outputs a signal to the CPU which discontinues the microsystem activity to service the interrupt. However, the microprocessor only knows that one of the OR-lines has requested service, not specifically which line. The microsystem must therefore scan the network to determine who actually needs service. This is usually done by polling each connected device in turn and asking if it is the interrupting device. A pseudo priority system is set up by the ordering of the polling, with the first device polled having the highest priority.

Multilevel interrupts. With multilevel interrupt capability each interrupting device is assigned its own interrupt line. In this manner, identification of the device requesting service

will be immediate because the microprocessor does not have to search for the device requesting the interrupt, as it knows which line requested the interrupt.

One limitation of this setup may be that the number of separate interrupt lines is usually very restricted (under ten), and any additional interrupting devices must be OR-tied to one of the previously used interrupt lines. Priority is usually set up such that those devices attached to one of the interrupt lines have priority over all other lines, a second line has priority over all other lines except the first, and so forth through all the lines.

Vectored interrupt. The fastest mode of interrupt operation is vectored interrupt. In this case, the interrupting device not only requests service, but its interrupt also causes a direct branch of the program to service the required interrupt. Thus, a vectored interrupt causes a branch immediately to the subprogram necessary to service it.

The three interrupt schemes presented, and no interrupts, play an important part in the responsiveness of microcomputer systems. As with most things, there is a cost-speed trade-off involved here. The higher the interrupt's speed and capability, the greater the cost. Some applications, by their very nature, must have high quality interrupts to work in real time -- no matter what the cost. Others may require no interterup at all.

4.2.9 Power Supply Considerations

The power supply consideration attribute may be stated as:

> Decide if the advantages of each remaining microsystem justify its power supply requirements and costs.

This attribute is one that is often overlooked by designers of microsystems, but is generally being recognized as gobbling up a substantial portion of a microsystem's budget. Several areas of concern should be addressed in this attribute:

1) Regulation required and the number of different voltages required
2) Environmental considerations

These are discussed in more detail in the following sections.

Regulation and the number of different voltages required. The importance of this key value is the direct relationship that occurs between it and size, complexity, and cost of the power supply necessary. As with any system, the more a power supply must do (the number of voltages needed) and the greater the quality (regulation required) of its work, the larger and more complex must its circuitry be, and the more it costs to design, build, and service it in the field.

Environmental considerations. Many microsystem applications

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provide extreme environmental factors which force rigid requirements on the size, weight, total power output, durability, and universal hookup capabilities of power supplies. There is a wide range of power requirements for individual microsystems, and each microsystem must be judged as acceptable (or unacceptable) in the light of environmental conditions facing it. If any of the microsystem's power requirements cannot be met within environmental restrictions, then it must be dropped from the contender list. If none of the microsystems will function within the environmental restrictions, one must reexamine the feasibility of using microsystems, or else somehow lessen the environmental restrictions.

Historically, power supplies have had secondary consideration in systems. With the diverse applications of microsystems, however, it must function as a first line consideration.

4.2.10 Timing Consideration

The tenth attribute in the selection algorithm, timing considerations, may be stated:

> Decide which clock frequencies, phases, and qualities are compatible with the design requirements, as this partly determines the speed and necessary circuit design for clock generator and timing.

Microsystem timing and clock generation methods affect the system because instruction times are based on maximum clock frequencies and cycle times. (e.g. It may be necessary to select a lower-frequency clock to optimize some system considerations, such as memory access time or clock generator synchronization with external timing.) Areas of concern in this attribute include the following key values:

1) Frequencies
2) Phase
3) Circuit Quality

Every microsystem needs some kind of synchronizing clock mechanism, and most of the MOS microsystems require two-phase clocks. In the simplest case the user need only supply a crystal or a series R-C network to establish the time constant of the on-chip clock. The manufacturer may also offer a special clock-generating chip. At the other extreme, some microsystems require a four-phase non-overlapping clock signal system.

Although all manufacturers publish a sample clock circuit for their chips, most of these are not practical to use in production because they have four interacting variable controls which must be adjusted for optimum pulse repetition-rate and width. The most common solution to this is the use of DIP-shaped crystal clocks available from other vendors. These

extra features all add to the final cost.

4.2.11 Low-Level Synthesis

Little more than mention will be made of this last attribute proposed, low level synthesis. The major reason for this omission being lack of space. All of the previous attributes have concerned themselves with the external features of the microsystems, and have eliminated those obvious mismatches. What is alluded to by low-level synthesis is a minutely detailed (i.e. register count and placement, bus interconnections, function segregation) architectural comparison of those remaining microsystem contenders with the user's design. Manually, this involves noting strict architectural inflexibilities in each contender microsystem which may not allow conformance to the user's design. For example, the registers of a contender microsystem may be permanently positioned (and interconnected) on a chip. If this interconnection scheme doesn't match the desired scheme, the contending microsystem must be eliminated; or else the user must work around the inflexibility.

With the above discussion in mind; one may begin at some internal point in his design and gradually perform an expanding synthesis until covering his entire architecture. While at each incremental expansion, compare all contending microsystems to the synthesis and discard mismatches. An operation such as this requires very detailed microsystem

specification and information. It is for this reason that the attribute appears last, after the other attributes have eliminated as many microsystems as possible.

CHAPTER 5

SUPPORTING THE ALGORITHM

5.1 MICROSYSTEM CATALOGUING

With the dramatic increase in the number of microsystems every day, it is becoming more and more difficult to maintain accurate records on available microsystems and their various options. This is true for the small volume users, since the microsystems manufacturers are reluctant to give detailed information about their product to other than large-order customers, and for large volume users because they are unable to efficently handle the bulk information they receive. In other words, most microsystems users have either too little information to select from, or else too much to sort through. For this reason, the cataloguing scheme proposed in this report is two-fold, as detailed below.

Microsystem catalogue. It is the purpose of the cataloguing scheme to first provide only the information required to narrow down the microsystem contender field to a more manageable number, and then to provide the more detailed material required for the subset of microsystems really in contention. This is done using a single-sheet outline, of the form found in Figure 21, which contains enough information to use with the first ten attributes. (i.e. These single-sheet outlines act as a data base containing all the key value information required to compare against the user's desired key value functions.) Appendix

Manufacturer.....
Model Number.....
Major Application.....
    Data Acquisition-Control..
    Data Communications.....
    Human Interface Equipment.
    Computational.....
    Other.....
Availability.....
    First Shipped.....
    Cost.....
Technology.....
Chip-Set Family Size.....
    Architecture.....
    Chips In CPU/Pins.....
    Peripheral Interfaces.....
    Special Purpose Chips.....
Software.....
    Resident Assembler.....
    Cross Assembler.....
    Monitor.....
    High Level Languages.....
    Instruction Simulator.....
    Prototyping System.....
    Reg. Load Time For Instr..
    Reg to Reg Add Time.....
    Number of Instructions....
        Arithmetic.....
        Logical.....
        Shift/Rotate.....
        Index Group.....
        Stack Control.....
        Other.....
Memory Requirements.....
    Microprogrammed.....
    DMA.....
Bus Sizes.....
    Data Path Width.....
    Address Path Width.....
Interrupt.....
Power Requirements.....
Timing Requirements.....

FIG. 21 STRUCTURE OF THE MICROSYSTEM SINGLE-SHEET OUTLINE

C contains a collection of these single-sheet outlines compiled by the author, as a guide to what today's microsystems offer. Once the top-down analysis of the first part of the cataloguing scheme is completed, and only a limited subset of the original contending microsystems is left; more detailed information on those microsystems remaining can be gathered for the low level synthesis attribute.

This two level method of cataloguing microsystems should help solve the problem of insufficient details for the small volume user, and the problem of too much bulk information for the large volume user by requiring the harder to get and handle detailed information on microsystems for only those microsystems which have proven themselves viable for the user's design.

5.2 AUTOMATING THE PROCESS

As the number of microsystems grows, even the single-sheet outline becomes too bulky to handle. The most obvious solution to this problem is the creation of a computerized data base which contains the required information in some standard form accessable to the computer as it needs it.

Catalogue automation. The data structure presented as an example in Chapter 3, Figure 3, could function well in a computer environment. The data base could be directly placed on the computer as an MxN matrix with the cell (m,n), residing at the intersection of row m and column n, representing the key value functional representation for the m^{th} microsystem and the n^{th}

attribute. A data base structure on this theme would have all the easy entry, viewing, manageability, and accessibility advantages of the typical computer data base.

Low level synthesis automation. In Chapter 4, mention was made of comparing the architectures of contending microsystems with the user's design in order to determine the best architectural fit. By hand this proves to be a very arduous task, and a prime candidate for automation techniques. Presented below is an intuitive approach to automating the low level synthesis.

It is believed that the architecture of a microsystem may be represented as a tree (or digraph) with distinctive nodal types representing the registers, ALU, and other similar structures. The branches would represent the interconnective buses; with a distinction being made between internal-to-chip, rigidly connected buses and those buses user-alterable by designating them strong links and weak links respectively. Each microsystem could be represented by its own distinctive tree and stored with the data base.

An architectural fit would be defined as the correct formation of the desired architecture (by a contending microsystem) by node grouping without breaking any strong links.

Algorithm automation. Once the data base and the low level synthesis attribute have been placed on the computer, the whole algorithm shows itself amenable to the same computer environment. The data structure of Figure 3 presents those basic storage elements required, and the MS Algorithm could easily

be implemented in some high level language (e.g. FORTRAN).

5.3 SUMMARY

A microsystem selection algorithm has been defined and presented with emphasis placed on completeness, definiteness, modularity and modifiability, and reliability. It has been shown that this algorithm is in response to a very real need for some order to be injected into the selection process.

Attributes, and their associated key values, have been suggested and described in some detail to impart some understanding into those areas important to selection.

Appendices such as the vendor index, bibliography of microsystem articles, and single-sheet outlines have been included to provide a single source for much of the required data for microsystem selection.

The following areas should be considered in future studies of microsystem selection:

1) Low level synthesis should be studied in more detail and a low level synthesis program should be constructed.
2) Work should be done in forming a microsystem data base before the influx of microsystems generates too much new information to handle.

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GLOSSARY

ACCESS TIME
The time interval between a request for information and its actual availability.

ACCUMULATOR
A device which stores a value, and when receiving another value adds them together.

ADDRESS
An expression which designates a special cell, or location, in a memory device.

ALGORITHM
A term used by mathematicians to describe a set of procedures by which a result may be obtained.

ALU
Arithmetic Logic Unit, a portion of a system which does the arithmetic and logic operations.

ASSEMBLER
A computer program which prepares a machine language program from another higher level language program by substituting binary (absolute) operation codes for symbolic codes.

ASYNCHRONOUS
To operate independent of timing considerations from another part of the system.

BENCHMARK PROGRAM
A program used to evaluate the performance of software by comparison of how each machine handles exactly the same problem.

BINARY
This term refers to the base 2 number system.

BIPOLAR
The most popular fundamental kind of IC, formed by layers of silicon with differing electrical properties.

BIT
A single piece of information, or binary place holder, representing either true or false (1 or 0) which can be combined with other bits to build words.

BLOCK DIAGRAM
A diagram of a system in which the major parts are represented by geometric figures, with interconnections to show the basic functional relationships among the parts.

BOOTSTRAP
A technique or device designed to start itself.

BRANCHING
The process of selecting where to get the next operation from on the basis of different results.

BUS
One or more connective lines for transmitting signals and power.

CHIP
A small piece of material impregnated with impurities so as to form circuits.

CMOS
Complementary MOS refers to a combination of p-channel and n-channel transistors which results in a fast, low-power technology.

CODE
A set of unambiguous rules specifying the way in which data may be represented and interpreted.

COMPILER
A program that prepares a machine language program from a computer program written in another computer language by generating appropriate machine instructions and assembling them.

CPU
Central processing unit, part of a computer system which contains main storage, ALU, and registers to perform ALU operations, generate control signals and other bookkeeping operations.

DCTL
Direct coupled transistor logic, an early form of bipolar logic on which I^2L is based.

DEBUG
To detect and locate mistakes from a program.

DIP
Dual in-line package, the case surrounding a chip whose name refers to the double, parallel rows of pins which connect the chip to the circuit board. A DIP is also referred to as a bug.

DMA
Direct memory access, is a method of I/O for a system that

uses a special controller whose sole responsibility is to move data into and out of the memory without program intervention.

DTL
The first successful logic family, now replaced by TTL.

ECL
Emitter-coupled logic circuits, bipolar technology also known as current mode logic, the fastest logic family known today (1nsec delay/gate is possible).

EDIT
To modify the format of data so as to improve its contents.

EMULATE
To imitate, or copy, the performance of one system by another such that the imitator can handle the original programs without modification.

FLOW CHART
A graphic representation used for problem definition, analysis, and/or solution; symbols are used to show operations, data flow, equipment, and decisions.

HARDWARE
The physical equipment made up of mechanical, electrical or electronic devices.

HARVARD
Harvard architecture refers to the fact that the program and data are stored in separate memories & can't be mixed.

HYBRIDS
Circuits fabricated by interconnection of smaller circuits of different technologies mounted on a single substrate.

IC
Integrated circuits, a complex electrical circuit fabricated on a single piece of material (typically this material is silicon).

INTERFACE
An interface is a point of contact, or interaction, between two, or more, elements of a system.

INTERRUPT
To stop a process to perform another task which, when completed, restarts the interrupted task.

I/O

Input/Output, is the hardware by which information enters and leaves the system.

LANGUAGE
A set of symbols, conventions, and rules used to convey information.

LIFE CYCLE
The full history of a product from its introduction to its removal from the market.

LSI
Large-scale integration, is the use of large-area chips and high packing density; usually considered the lower limit.

MACHINE CODE
A basic operation code, using 1's and 0's, that a machine is designed to recognize.

MASK
A pattern of characters, or filter, used to control the retention or elimination of portions of another pattern.

MICROPROGRAMMING
Control technique using stored programs to emulate typically hardware functions.

MOS
Metal-oxide-semiconductor, an active semiconductor device in which a conducting channel is induced in the region between two electrodes by a voltage applied to an insulated electrode on the surface of the region.

MSI
Medium scale integration, usually refers to chips with 50-100 components.

MULTIPLEX
To transmit two or more messages on the same channel using some appropriate message mixing routine.

NMOS
Negative channel MOS, refers to MOS of negative-charge currents (operates at twice the speed of PMOS).

PLA
Programmable logic array, is an IC that employs ROM matrices to combine sum and product terms of logic networks, and thus perform logic sequences.

PRINCETON

Princeton (or Von Neumann) arch. refers to the fact that prog. & data are stored in same mem: can modify instruct.

PRIORITY
A form of precedence where one action is performed before another.

PMOS
Positive channel MOS, refers to the oldest type of MOS where electric current consists of flow of positive charges.

PROM
Programmable read only memory, a read only semiconductor memory element which can be programmed after packaging by use of special techniques (and usually erasable under UV light).

PROPAGATION DELAY
The time required to proceed through the inherent delay within logic levels.

PUSHDOWN STACK
A register which constructs and maintains a series of items in such a manner that the last item in is the first out.

RAM
Random access memory, a fast memory from which information can be addressed and obtained randomly, without sequential searching.

REAL TIME
Performance of a computation at the actual time the physical event is occurring.

REGISTER
A special storage location for fast temporary storage.

ROM
Read only memory, a fixed program semiconductor storage element that is preprogrammed at manufacture time.

SIMULATOR
A device that represents certain features of the behavior of a system such that the behavior may be more easily studied.

SOFTWARE
The set of computer programs and documentation which functions to control the hardware elements in such a way as to perform a given task.

SOS

Silicon on sapphire refers to the layers of material which achieve high speed (equal to some bipolar speeds) through MOS technology by insulation of the components.

TTL

Bipolar semiconductor transistor-transistor logic.

VOLATILE STORAGE

A storage medium in which stored data is lost which the power is removed.

WORD

A string of bits collectively considered as an entity.

Ref. [3, 5, 13]

APPENDIX A

VENDOR INDEX

Advanced Micro Devices
901 Thompson Rd.
Sunnyvale, California 94086
(408)732-2400

American Microsystems, Inc.
3800 Homestead Rd., Santa Clara, CA 95051
Established 1966
Gross sales $58M
David L. Gellatly, mkt mgr (408)255-3651

Applied Computing Technology
17961 Sky Park Cir., Irvine, CA 92707
Established 1972; 15 employees
Gross sales $400K
Neil Gleason, dir mktg (714)557-9972

Burroughs
P.O. Box 517
Paoli, Pennsylvania 19301
(215)648-2000

Computer Automation, Inc.
18651 VonKarman Ave., Irvine, CA 92664
Gross sales not released.
D. Bush, mgr mktg serv (714)833-3380

Comstar Corp.
7413 Washington, S. Minn., MN 55435
Gross sales not released.
Vern Carlson, natl sls mgr (612)941-4454

Control Logic Inc.
9 Tech. Cir., Natick, MA 01760
Subsidiary of harnischfeger Corp.
Established 1961; 60 employees
Gross sales $1.5M
Geoff Hawkes, sls mgr (617)655-1170

Data Architects, Inc.
460 Totten Pond Rd., Waltham, MA 02154
Established 1967; 150 employees
Gross sales $3.2M
Thomas Gehman, sr engr (617)890-7730

Digital Equipment Corp.
One Iron Way, Marlborough, MA 01720
Established 1974; 200 employees
Gross sales not released.
Peter Connell, pro supv (617)481-7400

Digital Laboratories

377 Putnam Ave., Cambridge, MA 02139
Established 1971
Gross sales not released.
William M. Kahn, chf engr (617)876-6220

Dynamic Data Systems Corp.
533 Stevens Ave., Solana Bch, CA 92075
Established 1973; 30 employees
Gross sales not released.
Lee Houser, sls mgr (714)755-5161

Electronic Arrays
550 Middlefield Rd.
Mountain View, CA 94043
(415)964-4321

Fabri-Tek Inc.
5901 S. County Rd. 18, Minn, MN 55436
Established 1957; 2,500 employees
Gross sales over $39M
Karl Kulp, prod mgr (612)935-8811

Fairchild Semiconductor
464 Ellis St., Mt View, CA 94042
Subsidiary of Fairchild Camera & Inst.
Gross sales not released.
Contact local sales office.

General Automation, Inc.
1055 S. East St., Anaheim, CA 92805
Established 1967; 1,450 employees
Gross sales $62M
John Dillon, pub mgr (714)778-4800

General Instruments
600 W. John St., Hicksville, NY 11802
2,000 employees
Gross sales $45M
Sales office (516)733-3097

Intel Corp.
3065 Bowers Ave., Santa Clara, CA 95051
Gross sales not released.
Hal Feeney, mgr mktg (408)246-7501

International Marketing Services
52 Garden Road
Wellesley, Mass. 02181

Intersil Inc.
10900 N. Tantau Ave., Cupertino, CA 95014
Established 1969; 850 employees

Gross sales $24.6M
Hash M. Patel, mkt dir (408)257-5450

Microdata Corp.
17481 Red Hill Ave., Irvine, CA 92705
Established 1967; 450 employees
Gross sales $14M
R. C. Stack, mgr mkt commo (714)540-6730

Microsystems International Ltd.
P.O. Box 3529 Station C
Ottawa, Canada KIY, 4JI

Monolithic Memories, Inc.
1165 E. Arques Ave., Sunnyvale, CA 94086
Established 1969; 520 employees
Gross sales not released.
Dale Williams, dir mktg (408)739-3535

Mostek
1215 W. Crosby Rd., Carrollton, TX 75006
Established 1969; 2,000 employees
Gross sales $41M
Ken Davis, microproc mgr (214)242-0444

Motorola Semiconductor Products
5005 E. McDowell, Phoenix, AZ 85062
Information on sales and employees not released.
Van Lewing, micro mktg mgr (602)244-6228

National Semiconductor Inc.
2900 Semiconductor, Santa Clara CA 95051
Established 1959; 16,000 employees
Gross sales $213M
Philip Roybal, mkt mgr (408)732-5000

Process Computer Systems (PCS)
5467 Hill 23 Dr., Flint, MI 48507
Established 1968; 90 employees
Gross sales $3M
Bill Bowling, sls mgr (313)744-0225

Pro-Log Corp.
852 Airport Rd., Monterey, CA 93940
Established 1972; 23 employees
Gross sales $800K
Edwin Lee, president (408)372-4593

Raytheon Semiconductor
350 Ellis St.
Mountain View, CA
(415)968-9211

RCA Solid-State Div.
Route 202, Somerville, NJ 08876
Gross sales not released.
Dr. Lee Wu (201)722-3200

R2E Micro Computers
38 Garden Rd., Wellesley Hills, MA 02181
Established 1970; 115 employees
Gross sales $3.5M
M. W. Rohrbach, exec vp (617)235-3130

Rockwell Microelectronic Device Div.
3310 Miraloma Ave., Anaheim, CA 92803
Subsidiary of Rockwell International Corp.
Established 1970; # of employees not given
Gross sales not released.
R. F. Voigt, dir cust serv (714)632-3729

Scientific Micro Systems
520 Clyde Ave., Mt. View, CA 94043
Subsidiary of Corning Glass Works
Established 1969; 60 employees
Gross sales not released.
M. Liccardo, prod mgr (415)964-5700

Signetics Corp.
811 E. Arques Ave., Sunnyvale, CA 94086
Subsidiary of Corning Glass Works
Established 1962; 7,500 employees
Gross sales $98M
George Rigg, mgr MOS (408)739-7700

Standard Logic, Inc.
2215 S. Standard Ave., Santa Ana, CA 92707
Established 1967; 160 employees
Gross sales $3.7M
N. G. Compton, vp (714)979-4770

Teledyne Systems Co.
19601 Nordhoff St., Northridge, CA 91324
Subsidiary of Teledyne, Inc.
Established 1960; 1,500 employees
Gross sales $2,000M (corporate)
Frank Redding, prod mgr (213)886-2111

Texas Instruments Inc.
P.O. Box 1443
Houston, Texas 77001
(713)494-5115

Three Phoenix Co.
10632 N. 21st Ave., Phoenix, AZ 85029

Information on sales and employees not released.
John C. Dahl (602)944-2223

Transitron
168 Albion St.
Wakefield, MA 01880
(617)245-4500

Toshiba Transistor Works
1-Komukai
Toshiba-Cho
Kawasaki-Chi, Japan

Varitel Inc.
8857 Olympic, Beverly Hills, CA 90211
Established 1973; 7 employees
Gross sales $180K
Bruce Gladstone, president (213)659-5914

Warner & Swasey Electronic Products Division
30300 Solon Industrial Parkway
Solon, Ohio 44139

Western Digital Corp.
3128 Red Hill, Newport Beach, CA 95051
Established 1970; 700 employees
Gross sales $13.5M
G. Des Rochers, appl engr (714)557-3550

Xerox Corporation
Dept. 15-02
701 S. Aviation Blvd.
El Segundo, CA 90245
(213)679-4511

APPENDIX B

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A. R. Ward [15]

APPENDIX C

MICROPROCESSORS

Manufacturer	AMI
Model Number	S6800
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Single Sourced
First Shipped	1/75
Cost For Lots of 100	
Technology	NMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	through adaptor
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	no
High Level Languages	no
Instruction Simulator	no
Prototyping System	to be announced
Reg. Load Time For Instr.	2usec (8 bits)
Reg to Reg Add Time	2usec (8 bits)/to mem 2usec
Number of Instructions	72 (8, 16, 24 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	
Microprogrammed	yes
DMA	
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	standard
Power Requirements	
Timing Requirements	1MHz/2-phase

Manufacturer	Burroughs
Model Number	MINI-D
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1973
Cost For Lots of 100	$60
Technology	PMOS
Chip-Set Family Size	
Architecture	8-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	9usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	1 x 8 stack
Other	
Memory Requirements	256 words
Microprogrammed	no
DMA	no
Bus Sizes	8/12 bits
Data Path Width	
Address Path Width	
Interrupt	no
Power Requirements	-12, +5
Timing Requirements	

Manufacturer	Electronic Arrays
Model Number	
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1975
Cost For Lots of 100	
Technology	NMOS
Chip-Set Family Size	
Architecture	8-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	7 x 16 stack
Other	
Memory Requirements	64K words
Microprogrammed	no
DMA	yes
Bus Sizes	8/8 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	+5, +12
Timing Requirements	

Manufacturer	Fairchild
Model Number	F8
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	$75
Technology	NMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	2 chips/40 pins
Peripheral Interfaces	none
Special Purpose Chips	Clock Driver
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	2usec (8 bits)
Reg to Reg Add Time	2usec (8 bits)/to mem 5usec
Number of Instructions	101 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	64K words
Microprogrammed	yes
DMA	yes
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	chain
Power Requirements	+5, +12
Timing Requirements	2MHz/2-phase

Manufacturer	Fairchild
Model Number	PPS-25
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	2nd Quarter 1971
Cost For Lots of 100	$60
Technology	PMOS
Chip-Set Family Size	
Architecture	4-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	4 x 12 stack
Other	
Memory Requirements	6656 words
Microprogrammed	no
DMA	no
Bus Sizes	4 x 25/12 bits
Data Path Width	
Address Path Width	
Interrupt	no
Power Requirements	-9, +5
Timing Requirements	

Manufacturer.....	General Instruments
Model Number.....	CP1600
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	1/75
Cost For Lots of 100.....	
Technology.....	NMOS
Chip-Set Family Size.....	
Architecture.....	16 bit parallel
Chips In CPU/Pins.....	1 chip/40 pins
Peripheral Interfaces.....	none
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	yes
Prototyping System.....	no
Reg. Load Time For Instr..	2.4usec (16 bits)
Reg to Reg Add Time.....	2.4usec (16 bits)/to mem 3.2usec
Number of Instructions....	68 (16 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	
Memory Requirements.....	
Microprogrammed.....	yes
DMA.....	
Bus Sizes.....	16 bits
Data Path Width.....	16 bits
Address Path Width.....	separate 16 bits
Interrupt.....	nested
Power Requirements.....	
Timing Requirements.....	5MHz/2-phase

Manufacturer.....	Intel
Model Number.....	3000 Series
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	Double Sourced
First Shipped.....	7/74
Cost For Lots of 100.....	
Technology.....	bipolar
Chip-Set Family Size.....	
Architecture.....	2 bit slice, parallel
Chips In CPU/Pins.....	1 chip/28 pins
Peripheral Interfaces.....	none
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	no
Cross Assembler.....	cross microassemb.
Monitor.....	no
High Level Languages.....	no
Instruction Simulator.....	no
Prototyping System.....	no
Reg. Load Time For Instr..	150nsec (16 bits)
Reg to Reg Add Time.....	300nsec (16 bits)/to mem varys
Number of Instructions....	variable
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	
Memory Requirements.....	
Microprogrammed.....	user microprogram
DMA.....	
Bus Sizes.....	variable
Data Path Width.....	variable
Address Path Width.....	variable
Interrupt.....	vectored priority
Power Requirements.....	
Timing Requirements.....	8MHz/1-phase

Manufacturer	Intel
Model Number	3001
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	3rd Quarter 1974
Cost For Lots of 100	$550
Technology	bipolar
Chip-Set Family Size	
Architecture	2-bit slice
Chips In CPU/Pins	
Peripheral Interfaces	yes
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	16.5usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(NONE)
Other	
Memory Requirements	512 words
Microprogrammed	yes
DMA	yes
Bus Sizes	2N/18+
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	5
Timing Requirements	

Manufacturer	Intel
Model Number	MCS 4004
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	3/71
Cost For Lots of 100	less than $99
Technology	PMOS
Chip-Set Family Size	
Architecture	4 bit parallel
Chips In CPU/Pins	1 chip/16 pins
Peripheral Interfaces	display
Special Purpose Chips	Clock Driver
Software	resident bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	10.8usec (8 bits)
Reg to Reg Add Time	10.8usec (4 bit)/to mem 10.8usec
Number of Instructions	46 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	3 x 12 stack
Other	
Memory Requirements	4K words
Microprogrammed	no
DMA	no
Bus Sizes	4 bits
Data Path Width	4 bits
Address Path Width	separate 4 bits
Interrupt	no
Power Requirements	15 or (-10, +5)
Timing Requirements	750KHz/2-phase

Manufacturer	Intel
Model Number	4040
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	9/74
Cost For Lots of 100	less than $99
Technology	PMOS
Chip-Set Family Size	
Architecture	4 bit parallel
Chips In CPU/Pins	1 chip/24 pins
Peripheral Interfaces	display
Special Purpose Chips	Clock Driver
Software	resident bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	8usec (8 bits)
Reg to Reg Add Time	8usec (4 bits)/to mem 8usec
Number of Instructions	60 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	7 x 12 stack
Other	
Memory Requirements	4K words
Microprogrammed	no
DMA	no
Bus Sizes	4 bits
Data Path Width	4 bits
Address Path Width	separate 4 bits
Interrupt	vectored
Power Requirements	15 or (-10, +5)
Timing Requirements	1MHz/2-phase

Manufacturer	Intel
Model Number	8008/8008-1
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	12/71, 9/72
Cost For Lots of 100	less than $250
Technology	PMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/18 pins
Peripheral Interfaces	I/O port
Special Purpose Chips	Clock Driver
Software	resident bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	PL/M
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	20/12.5usec (8 bits)
Reg to Reg Add Time	20/12.5usec (8 bits)/to mem 32/ 20usec
Number of Instructions	48 (8 bits)
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	7 x 14 stack
Other	
Memory Requirements	16K words
Microprogrammed	no
DMA	no
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	vectored
Power Requirements	-9, +5
Timing Requirements	500/800KHz/2-phase

Manufacturer	Intel
Model Number	8080
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	12/73
Cost For Lots of 100	less than $400
Technology	NMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	I/O port
Special Purpose Chips	Clock Driver
Software	resident bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	PL/M
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	2.5usec (8 bits)
Reg to Reg Add Time	2usec (8 bits)/to mem 3.5usec
Number of Instructions	78 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	64K words
Microprogrammed	no
DMA	yes
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	vectored
Power Requirements	-5, +5, +12
Timing Requirements	2MHz/2-phase

Manufacturer	Intersil
Model Number	IM 6100
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	$175
Technology	CMOS
Chip-Set Family Size	
Architecture	12 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	tty
Special Purpose Chips	Clock Driver
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	
Reg to Reg Add Time	no released/to mem 5usec
Number of Instructions	50 (12 bits)
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	Modifies Program
Other	
Memory Requirements	4K words
Microprogrammed	yes
DMA	yes
Bus Sizes	12 bits
Data Path Width	12 bits
Address Path Width	separate 12 bits
Interrupt	yes
Power Requirements	5
Timing Requirements	2MHz/1-phase

Manufacturer.....	Monolithic
Model Number.....	6701
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	7/74
Cost For Lots of 100.....	$95/$600
Technology.....	bipolar
Chip-Set Family Size.....	
Architecture.....	4 bit slice, parallel
Chips In CPU/Pins.....	24 chips/40 pins
Peripheral Interfaces.....	no
Special Purpose Chips.....	
Software.....	bundled
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	no
Prototyping System.....	yes
Reg. Load Time For Instr..	1.2usec (16 bits)
Reg to Reg Add Time.....	900nsec (16 bits) to mem/1.2us
Number of Instructions....	22 (16 bits)
Arithmetic.....	no BCD
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	(NONE)
Other.....	
Memory Requirements.....	
Microprogrammed.....	user microprogram
DMA.....	no
Bus Sizes.....	16 bits
Data Path Width.....	16 bits
Address Path Width.....	separate 16 bits
Interrupt.....	1 level, priority opt.
Power Requirements.....	+5
Timing Requirements.....	5MHz/1-phase

Manufacturer	Mostek
Model Number	5065
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1st Quarter 1974
Cost For Lots of 100	$58
Technology	PMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	no
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	no
Prototyping System	no
Reg. Load Time For Instr.	8.5usec (8 bits)
Reg to Reg Add Time	10usec (8 bits)/to mem 10usec
Number of Instructions	51 (8/16 bits)
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	32K words
Microprogrammed	no
DMA	yes
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	priority
Power Requirements	-12, -5, +5
Timing Requirements	1.4MHz/3-phase

Manufacturer	Motorola
Model Number	M6800
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	7/74
Cost For Lots of 100	$150
Technology	NMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	through adaptor
Special Purpose Chips	
Software	unbundled
Resident Assembler	no
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	
Reg to Reg Add Time	not released/to mem 2 usec
Number of Instructions	72 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	64K words
Microprogrammed	yes
DMA	no
Bus Sizes	16 bits
Data Path Width	16 bits
Address Path Width	separate 16 bits
Interrupt	yes
Power Requirements	5
Timing Requirements	1MHz/2-phase

Manufacturer	National
Model Number	CMP-8
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	2nd Quarter 1975
Cost For Lots of 100	
Technology	NMOS
Chip-Set Family Size	
Architecture	8- bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	yes
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	1.6usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	64K words
Microprogrammed	no
DMA	yes
Bus Sizes	8/8 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	
Timing Requirements	

Manufacturer	National
Model Number	GPC/P
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1973
Cost For Lots of 100	$150
Technology	PMOS
Chip-Set Family Size	
Architecture	4-bit slice
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	14usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	16 x 4N stack
Other	
Memory Requirements	100 words
Microprogrammed	yes
DMA	yes
Bus Sizes	4N/23 bits
Data Path Width	
Address Path Width	
Interrupt	no
Power Requirements	-12, +5
Timing Requirements	

Manufacturer	National
Model Number	IMP-4
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	4th Quarter 1974
Cost For Lots of 100	$150
Technology	PMOS
Chip-Set Family Size	
Architecture	4-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	yes
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	12usec
Number of Instructions	
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	7 x 12 stack
Other	
Memory Requirements	4096 words
Microprogrammed	yes
DMA	no
Bus Sizes	4/4 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	-12, +5
Timing Requirements	

Manufacturer	National Semiconductor
Model Number	IMP-8A/500D
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	Double Sourced
First Shipped	3/74
Cost For Lots of 100	$181
Technology	PMOS
Chip-Set Family Size	
Architecture	4 bit slice, parallel
Chips In CPU/Pins	3 chips/24 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	no
Prototyping System	yes
Reg. Load Time For Instr.	11.2usec (8 bits)
Reg to Reg Add Time	4.2usec (8 bits)/to mem 11.2us
Number of Instructions	38 (8 bits)
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	16 x 8 stack
Other	
Memory Requirements	64K words
Microprogrammed	user microprogram
DMA	yes
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	yes
Power Requirements	-12, +5
Timing Requirements	715KHz/4-phase

Manufacturer	National
Model Number	IMP-16
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1973
Cost For Lots of 100	$310
Technology	PMOS
Chip-Set Family Size	
Architecture	16-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	4.6usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	16 x 16 stack
Other	
Memory Requirements	64K words
Microprogrammed	yes
DMA	yes
Bus Sizes	16/16 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	-12, +5
Timing Requirements	

Manufacturer	RCA
Model Number	COSMAC
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	$300
Technology	CMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	2 chips/28,40 pins
Peripheral Interfaces	no
Special Purpose Chips	
Software	unbundled
Resident Assembler	no
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr	6usec (8 bits)
Reg to Reg Add Time	18usec (8 bits)/to mem 6usec
Number of Instructions	59 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	7 x 16 stack
Other	
Memory Requirements	64K words
Microprogrammed	no
DMA	on-chip DMA facility
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	maskable
Power Requirements	5, -12
Timing Requirements	2.67MHz/1-phase

Manufacturer	Rockwell
Model Number	PPS-4
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1973 150K shipped
Cost For Lots of 100	approx. $45
Technology	PMOS
Chip-Set Family Size	
Architecture	4 bit parallel
Chips In CPU/Pins	1 chip/42 pins
Peripheral Interfaces	display, tty, gp
Special Purpose Chips	Clock Driver
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	4usec (8 bits)
Reg to Reg Add Time	4usec (8 bits)/to mem 4usec
Number of Instructions	50 (8 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	2 x 12 stack
Other	
Memory Requirements	4K words
Microprogrammed	yes
DMA	no
Bus Sizes	4 bits
Data Path Width	4 bits
Address Path Width	separate 4 bits
Interrupt	none
Power Requirements	17
Timing Requirements	200KHz/4-phase

Manufacturer	Rockwell
Model Number	PPS-8
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	10/74
Cost For Lots of 100	approx. $47
Technology	PMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/42 pins
Peripheral Interfaces	display, tty, gp
Special Purpose Chips	Clock Driver
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	5usec (8 bits)
Reg to Reg Add Time	4usec (8 bits)/to mem 5usec
Number of Instructions	109 (8, 16, 24 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	16K words
Microprogrammed	yes
DMA	yes
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	3 x 16 daisy chain
Power Requirements	17
Timing Requirements	250KHz/4-phase

Manufacturer	Signetics
Model Number	26501 "PIP"
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	$200
Technology	NMOS
Chip-Set Family Size	
Architecture	8 bit parallel
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	no
Special Purpose Chips	
Software	unbundled
Resident Assembler	no
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	no
Prototyping System	no
Reg. Load Time For Instr.	4.8usec (8 bits)
Reg to Reg Add Time	4.8usec (8 bits)/to mem 4.8usec
Number of Instructions	72 (8, 16, 24 bits)
Arithmetic	BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	8 x 15 stack
Other	
Memory Requirements	32K words
Microprogrammed	no
DMA	no
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	1-level vectored
Power Requirements	5
Timing Requirements	1.25MHz/1-phase

Manufacturer	Western Digital
Model Number	CP 1611/1621/1631
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	
Technology	NMOS
Chip-Set Family Size	
Architecture	8/16 bit parallel
Chips In CPU/Pins	3 chips/40 pins
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	no
High Level Languages	no
Instruction Simulator	no
Prototyping System	to be announced
Reg. Load Time For Instr.	900nsec (8 bits)
Reg to Reg Add Time	300nsec (8 bits)/to mem 1.2usec
Number of Instructions	over 80 (16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	
Microprogrammed	user microprogram
DMA	
Bus Sizes	8/16 bits
Data Path Width	8/16 bits
Address Path Width	separate 8/16 bits
Interrupt	priority, 4 level
Power Requirements	
Timing Requirements	3.3MHz/4-phase

Manufacturer	National
Model Number	PACE
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost For Lots of 100	$161
Technology	PMOS
Chip-Set Family Size	
Architecture	16-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	10usec
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	64K words
Microprogrammed	
DMA	
Bus Sizes	16/16 bits
Data Path Width	
Address Path Width	
Interrupt	
Power Requirements	+5, -12
Timing Requirements	

Manufacturer	Raytheon
Model Number	RP-16
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	4th Quarter 1974
Cost For Lots of 100	
Technology	bipolar
Chip-Set Family Size	
Architecture	4-bit slice
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	lusec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	64K words
Microprogrammed	yes
DMA	no
Bus Sizes	4N/48 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	5
Timing Requirements	

Manufacturer	Toshiba
Model Number	TLCS-12
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1974
Cost For Lots of 100	$215
Technology	NMOS
Chip-Set Family Size	
Architecture	12-bit CPU
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	13usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	4K words
Microprogrammed	yes
DMA	no
Bus Sizes	12/12 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	-5, +5
Timing Requirements	

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Manufacturer	Transitron
Model Number	TMC/1601
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	3rd Quarter 1975
Cost For Lots of 100	
Technology	bipolar
Chip-Set Family Size	
Architecture	4-bit slice
Chips In CPU/Pins	
Peripheral Interfaces	no
Special Purpose Chips	
Software	
Resident Assembler	
Cross Assembler	
Monitor	
High Level Languages	
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	.4usec
Number of Instructions	
Arithmetic	no BCD
Logical	
Shift/Rotate	
Index Group	
Stack Control	(RAM)
Other	
Memory Requirements	32K words
Microprogrammed	yes
DMA	yes
Bus Sizes	16/16 bits
Data Path Width	
Address Path Width	
Interrupt	yes
Power Requirements	
Timing Requirements	

MICROCOMPUTERS

Manufacturer.....	Applied Computing
Model Number.....	CBC-4/CBC-4N-Intel
Major Application.....	controllers
Data Acquisition-Control..	intelligent terminal
Data Communications.....	peripheral controller
Human Interface Equipment.	point of sale terminal
Computational.....	process controller
Other.....	heavy equipment
Availability.....	
First Shipped.....	11/72 119 shipped
Cost For Lots of 100.....	$495
Technology.....	PMOS
Chip-Set Family Size.....	12 chips/7 x 7" board
Architecture.....	4 bit PMOS
Chips In CPU/Pins.....	1 chip/16 pins
Peripheral Interfaces.....	no
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	no
Cross Assembler.....	no
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	30usec (4 bits)
Number of Instructions....	45 (8 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary
Memory Requirements.....	RAM-Intel spec 1.2K bits PMOS ROM-Intel stand 4K bits PMOS PROM-Intel stand 4K bits PMOS
Microprogrammed.....	no
DMA.....	no
Bus Sizes.....	maximum I/O channels 16
Data Path Width.....	4 bits
Address Path Width.....	shared with memory
Interrupt.....	no
Power Requirements.....	
Timing Requirements.....	

Manufacturer.....	Applied Computing
Model Number.....	UMPS-4-Rockwell
Major Application.....	intelligent terminal
Data Acquisition-Control..	intelligent terminal
Data Communications.....	peripheral controller
Human Interface Equipment.	point of sale terminal
Computational.....	process controller
Other.....	heavy equipment
Availability.....	
First Shipped.....	4/74 10 shipped
Cost For Lots of 100.....	$695
Technology.....	PMOS
Chip-Set Family Size.....	5 chips/5 x 7" board
Architecture.....	4 bit PMOS
Chips In CPU/Pins.....	1 chip/42 pins
Peripheral Interfaces.....	display, printer, gen. purpose
Special Purpose Chips.....	
Software.....	bundled
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	15usec (4 bits)
Number of Instructions....	50 (8 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary/decimal
Memory Requirements.....	RAM-Rockwell spec 4K bits PMOS ROM-Rockwell stand 16K bit PMOS PROM-Intel stand 16K bits PMOS
Microprogrammed.....	yes
DMA.....	one
Bus Sizes.....	maximum I/O channels 16
Data Path Width.....	4 bits
Address Path Width.....	shared with memory
Interrupt.....	no
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Computer Auto
Model Number	LSI-1-National custom
Major Application	
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	1/75
Cost For Lots of 100	$985-$2,020
Technology	PMOS
Chip-Set Family Size	70 chips/15 x 16.9" board
Architecture	16 bit PMOS
Chips In CPU/Pins	7 chips/40 pins
Peripheral Interfaces	disp, tty, paper tape, card
Special Purpose Chips	read, print, mag tape
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	9.2usec (16 bit)
Number of Instructions	168 (16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 512K bits PMOS ROM-stand 512K bits PMOS PROM-stand 512K bits PMOS
Microprogrammed	yes
DMA	yes
Bus Sizes	maximum I/O channels 248 (16 b)
Data Path Width	16 bits
Address Path Width	shared with memory
Interrupt	vectored
Power Requirements	
Timing Requirements	

Manufacturer	Comstar
Model Number	System 4-Intel
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	process controller
Other	traffic cont, calc
Availability	
First Shipped	
Cost For Lots of 100	$950
Technology	PMOS
Chip-Set Family Size	1-36 chips/4.5 x 4.5" board
Architecture	4 bit PMOS
Chips In CPU/Pins	1 chip/16 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	unbundled
Resident Assembler	no
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	10.8usec (4 bits)
Number of Instructions	45 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary/decimal
Memory Requirements	RAM-spec 20.58K bits PMOS ROM-stand 256 bits bipolar PROM-stand 2.048K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	maximum I/O channels 64 (4 bit)
Data Path Width	4 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer	Control Logic
Model Number	L Series-Intel 8008/8008-1
Major Application	controllers
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	process controller
Other	test equipment
Availability	
First Shipped	1/73 200 shipped
Cost For Lots of 100	$335
Technology	PMOS
Chip-Set Family Size	2-12 chips/4.8 x 3.2" board
Architecture	8 bit PMOS
Chips In CPU/Pins	24 chips/18 pins
Peripheral Interfaces	tty, display EIA RS-232-C
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	20/12.5usec (8 bits)
Number of Instructions	48 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 16K bits PMOS ROM- PROM-stand 16K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	maximum I/O channels 32 (8 bit)
Data Path Width	4 bits
Address Path Width	separate 4 bits
Interrupt	8 priority levels
Power Requirements	
Timing Requirements	

Manufacturer	Control Logic
Model Number	Mighty Micro-Intel 8080
Major Application	control, test
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	process controller
Other	
Availability	
First Shipped	10/74
Cost For Lots of 100	$495
Technology	NMOS
Chip-Set Family Size	2-16 chips/4.8 x 3.2" board
Architecture	8 bit NMOS
Chips In CPU/Pins	20 chips/40 pins
Peripheral Interfaces	tty, EIA RS-232-C
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr	
Reg to Reg Add Time	2.0usec (8 bits)
Number of Instructions	78 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 64K bits NMOS ROM- PROM-stand 64K bits NMOS
Microprogrammed	no
DMA	no
Bus Sizes	maximum I/O channels 256 (8 b)
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	8 level priority
Power Requirements	
Timing Requirements	

Manufacturer.....	Data Architects
Model Number.....	CM 101-Intel MCS-4
Major Application.....	pay tv controller
Data Acquisition-Control..	no
Data Communications.....	peripheral controller
Human Interface Equipment.	no
Computational.....	process controller
Other.....	
Availability.....	
First Shipped.....	9/73 16 shipped
Cost For Lots of 100.....	$1,420
Technology.....	PMOS
Chip-Set Family Size.....	92 chips/13.10 x 6.88" board
Architecture.....	4 bit PMOS
Chips In CPU/Pins.....	1 chip/16 pins
Peripheral Interfaces.....	tty
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	no
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	12.6usec (4 bits)
Number of Instructions....	45 (8, 16 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary/decimal
Memory Requirements.....	RAM-stand/spec 4K bit PMOS,NMOS ROM-stand/spec 4K bit PMOS,NMOS PROM-stand/spec 4K bits PMOS
Microprogrammed.....	no
DMA.....	no
Bus Sizes.....	maximum I/O channels 32 (4 bit)
Data Path Width.....	4 bits
Address Path Width.....	separate 4 bits
Interrupt.....	polling
Power Requirements.....	
Timing Requirements.....	

Manufacturer.....	Digital Equip
Model Number.....	Kit 8/A-TTL design
Major Application.....	PDP 8/E compat
Data Acquisition-Control..	intelligent terminal
Data Communications.....	peripheral controller
Human Interface Equipment.	point of sale terminal
Computational.....	process controller
Other.....	
Availability.....	
First Shipped.....	
Cost For Lots of 100.....	$895
Technology.....	bipolar
Chip-Set Family Size.....	
Architecture.....	12 bit bipolar
Chips In CPU/Pins.....	
Peripheral Interfaces.....	tty, display
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	yes
High Level Languages.....	yes
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	3usec (12 bits)
Number of Instructions....	--(12 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary
Memory Requirements.....	RAM-stand 384K bits NMOS ROM-stand 384K bits NMOS PROM-stand 384K bits NMOS
Microprogrammed.....	no
DMA.....	yes
Bus Sizes.....	maximum I/O channels 64 (12 b)
Data Path Width.....	12 bits
Address Path Width.....	shared with memory
Interrupt.....	yes
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Digital Equip
Model Number	MPS Series-Intel 8008
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	4/74
Cost	$410
Technology	PMOS
Chip-Set Family Size	
Architecture	8 bit PMOS
Chips In CPU/Pins	1 chip/18 pins
Peripheral Interfaces	
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	10usec (8 bits)
Number of Instructions	48 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 32K bits NMOS ROM- PROM-stand 32K bits NMOS
Microprogrammed	no
DMA	no
Bus Sizes	maximum I/O channels 256 (8 b)
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	yes
Power Requirements	
Timing Requirements	

Manufacturer	Digital Labs
Model Number	PB-96-TTL design
Major Application	control and acquis.
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	3/74
Cost	$685-$1,155
Technology	bipolar
Chip-Set Family Size	72-82 chips/9 x 15" board
Architecture	8 bit bipolar
Chips In CPU/Pins	72 chips
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	2.9usec (8 bits)
Number of Instructions	18 (8, 16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand/spec 512K bits ROM-stand 512K bits PROM-stand 8K bits
Microprogrammed	yes
DMA	no
Bus Sizes	maximum I/O channels 12 (8 bit)
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer	Dynamic Data Systems
Model Number	DD-4i-Intel 4004
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	9/73 160 shipped
Cost	$499
Technology	PMOS
Chip-Set Family Size	not released/8.5 x 10.5" board
Architecture	4 bit PMOS
Chips In CPU/Pins	1 chip/16 pins
Peripheral Interfaces	
Special Purpose Chips	
Software	unbundled
Resident Assembler	no
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	22usec (4 bits)
Number of Instructions	46 (8, 16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand/spec .32K bits PMOS ROM-stand/spec 8K bits PMOS PROM-stand 8K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	max I/O channels 256 (4 bits)
Data Path Width	4 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer.....	Fabri-Tek
Model Number.....	MP12-TTL design
Major Application.....	process controller
Data Acquisition-Control..	intelligent terminal
Data Communications.....	peripheral controller
Human Interface Equipment.	point of sale terminal
Computational.....	process controller
Other.....	data acquisition
Availability.....	
First Shipped.....	8/74 30 shipped
Cost.....	$890-$1,340
Technology.....	bipolar
Chip-Set Family Size.....	130 chips/9 x 15" board
Architecture.....	12 bit bipolar
Chips In CPU/Pins.....	129 chips
Peripheral Interfaces.....	tty
Special Purpose Chips.....	
Software.....	bundled
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	not released
Number of Instructions....	40 (12 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary/ASCII
Memory Requirements.....	RAM-stand 48K bits core ROM-stand 2K bits bipolar PROM-stand 2K bits bipolar
Microprogrammed.....	user microprogram
DMA.....	yes
Bus Sizes.....	max I/O channels 63 (12 bits)
Data Path Width.....	12 bits
Address Path Width.....	shared with memory
Interrupt.....	single level
Power Requirements.....	
Timing Requirements.....	

Manufacturer	General Automation
Model Number	LSI 16-Rockwell custom
Major Application	SPC-16
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	not released
Cost	$1,350-$2,350
Technology	SOS/MOS
Chip-Set Family Size	145 chips/7.75 x 11" board
Architecture	16 bit SOS/MOS
Chips In CPU/Pins	2 chips/40 pins
Peripheral Interfaces	
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	yes
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	1.3usec (16 bits)
Number of Instructions	80 (16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 256K bits PMOS ROM-stand 256K bits bipolar PROM-stand 256K bits bipolar
Microprogrammed	no
DMA	yes
Bus Sizes	max I/O channels 64 (16 bits)
Data Path Width	16 bits
Address Path Width	separate 16 bits
Interrupt	vector
Power Requirements	
Timing Requirements	

Manufacturer	Intel
Model Number	IMM 4-42-Intel 4004
Major Application	controllers
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	not released
Cost	$395
Technology	PMOS
Chip-Set Family Size	not released/6.18 x 8" board
Architecture	4 bit PMOS
Chips In CPU/Pins	1 chip/16 pins
Peripheral Interfaces	tty, I/O port
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	10.8usec (4 bits)
Number of Instructions	46 (4 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 1.3K-10.2K PMOS ROM- PROM-stand 8K-32K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	max I/O channels 864 (4bits)
Data Path Width	4 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer	Intel
Model Number	8-82-Intel 8008
Major Application	terminals
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	instrumentation
Availability	
First Shipped	not released
Cost	$450
Technology	PMOS
Chip-Set Family Size	not released/6.18 x 8" board
Architecture	8 bit PMOS
Chips In CPU/Pins	1 chip/18 pins
Peripheral Interfaces	tty
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	PL/M
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	20usec (8 bits)
Number of Instructions	48 (8, 16, 24 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 128K bits PMOS ROM-stand 128K bits PMOS PROM-stand 128K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	max I/O channels 16
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer	Intel
Model Number	8-83-Intel 8080
Major Application	terminals
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	instrumentation
Availability	
First Shipped	not released
Cost	$590
Technology	NMOS
Chip-Set Family Size	not released/6.18 x 8" board
Architecture	8 bit NMOS
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	tty
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	PL/M
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	2.0usec (8 bits)
Number of Instructions	78 (8, 16, 24 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 512K bits PMOS ROM-stand 512K bits PMOS PROM-stand 512K bits PMOS
Microprogrammed	no
DMA	yes
Bus Sizes	max I/O channels 16
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	vectored
Power Requirements	
Timing Requirements	

Manufacturer	Microdata
Model Number	Micro-One-TTL design
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	process controller
Other	
Availability	
First Shipped	10/74
Cost	$636
Technology	bipolar
Chip-Set Family Size	95 chips/8.5 x 12" board
Architecture	8 bit bipolar
Chips In CPU/Pins	93 chips
Peripheral Interfaces	tty
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	BASIC, FORTRAN
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	5.28usec (8 bits)
Number of Instructions	107 (16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 256K bits PMOS ROM-stand 16K bits bipolar PROM-stand 16K bits bipolar
Microprogrammed	user microprogram
DMA	yes
Bus Sizes	max I/O channels 256 (8 bits)
Data Path Width	8 bits
Address Path Width	separate 8 bits
Interrupt	yes
Power Requirements	
Timing Requirements	

Manufacturer	National Semiconductor
Model Number	IMP-16C-National 16A/500D
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	no
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	6/73
Cost	$950
Technology	PMOS
Chip-Set Family Size	not released/8.5 x 11" board
Architecture	4 bit slice PMOS
Chips In CPU/Pins	5-6 chips/24 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	3usec
Reg to Reg Add Time	4.2usec (16 bits)
Number of Instructions	43-60 (16, 32 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 2K bits PMOS, NMOS ROM-stand 4K bits PMOS PROM-stand 4K bits PMOS
Microprogrammed	user microprogram
DMA	yes
Bus Sizes	max I/O channels 64 (16 bits)
Data Path Width	4 bit slice
Address Path Width	shared with memory
Interrupt	vectored
Power Requirements	5, 0, -12
Timing Requirements	715KHz

Manufacturer	Process Computer
Model Number	Micropac-Intel 8080
Major Application	process controller
Data Acquisition-Control	intelligent terminal
Data Communications	no
Human Interface Equipment	no
Computational	process controller
Other	
Availability	
First Shipped	1/74 20 shipped
Cost	$281-$3,000
Technology	NMOS
Chip-Set Family Size	20-40 chips/5 x 9.6" board
Architecture	8 bit NMOS
Chips In CPU/Pins	1 chip/40 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	3usec (8 bits)
Number of Instructions	78 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 32K bits NMOS ROM-stand 16K bits NMOS PROM-stand 2K bits NMOS
Microprogrammed	no
DMA	no
Bus Sizes	max I/O channels 256 (16 bits)
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	multi-level vector
Power Requirements	
Timing Requirements	

Manufacturer	Pro-Log
Model Number	PLS-400-Intel 4004
Major Application	terminals
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	process controller
Other	
Availability	
First Shipped	2/73 900 shipped
Cost	$395-$690
Technology	PMOS
Chip-Set Family Size	12-18 chips/4.5 x 6.5" board
Architecture	4 bit PMOS
Chips In CPU/Pins	var chips/16 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	bundled
Resident Assembler	no
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	30usec (4 bits)
Number of Instructions	47 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-spec 4K bits PMOS ROM-stand 4K bits PMOS, NMOS PROM-stand 4K bits PMOS
Microprogrammed	no
DMA	no
Bus Sizes	
Data Path Width	4 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer	Pro-Log
Model Number	MPS-800-Intel 8008
Major Application	controlled terminals
Data Acquisition-Control	yes
Data Communications	yes
Human Interface Equipment	no
Computational	yes
Other	
Availability	
First Shipped	1/74 30 shipped
Cost	$700-$1,500
Technology	PMOS
Chip-Set Family Size	30-100 chips/4.5 x 6.5" board
Architecture	8 bit PMOS
Chips In CPU/Pins	--/18 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	14usec (8 bits)
Number of Instructions	72 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 16K bits NMOS ROM-stand 16K bits PMOS, NMOS PROM-stand 16K bits PMOS
Microprogrammed	no
DMA	yes
Bus Sizes	
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	8 level priority
Power Requirements	
Timing Requirements	

Manufacturer	RZE Micro Comp
Model Number	Micral 1000 Series-Intel 8008, -1, 8080
Major Application	data acquisition
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	point of sale terminal
Computational	process controller
Other	
Availability	
First Shipped	4/73 350 shipped
Cost	$410-$1,250
Technology	PMOS, NMOS
Chip-Set Family Size	35-38 chips/3.5 x 7.5" board
Architecture	8 bit PMOS, NMOS
Chips In CPU/Pins	1 chip/18 pins
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	yes
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	12.5usec (8 bits)
Number of Instructions	74 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 8K bits ROM-stand 8K bits PROM-stand 8K bits
Microprogrammed	no
DMA	yes
Bus Sizes	max I/O channels 8 (8 bits)
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	priority
Power Requirements	
Timing Requirements	

Manufacturer.....	SMS
Model Number.....	200 Micro Cont-TTL design
Major Application.....	
Data Acquisition-Control..	intelligent terminal
Data Communications.....	peripheral controller
Human Interface Equipment.	no
Computational.....	process controller
Other.....	
Availability.....	
First Shipped.....	1/75
Cost.....	not released
Technology.....	bipolar
Chip-Set Family Size.....	9-61 chips/6.975" board
Architecture.....	8 bit bipolar
Chips In CPU/Pins.....	1 chip/53 pins
Peripheral Interfaces.....	
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	no
Cross Assembler.....	yes
Monitor.....	no
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	300nsec (8 bits)
Number of Instructions....	8 (16 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary
Memory Requirements.....	RAM-stand/spec 2K bits bipolar ROM-stand 65K bits bipolar PROM-stand 65K bits bipolar
Microprogrammed.....	no
DMA.....	no
Bus Sizes.....	
Data Path Width.....	8 bits
Address Path Width.....	separate 8 bits
Interrupt.....	no
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Standard Logic
Model Number	CASH-8-TTL design
Major Application	terminal controller
Data Acquisition-Control	intelligent terminal
Data Communications	peripheral controller
Human Interface Equipment	no
Computational	no
Other	
Availability	
First Shipped	2/74 50 shipped
Cost	$300-$595
Technology	bipolar
Chip-Set Family Size	52 chips/5 x 10" board
Architecture	16 bit bipolar
Chips In CPU/Pins	52 chips
Peripheral Interfaces	tty, display
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	200nsec (8 bits)
Number of Instructions	52 (16 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-spec 1K PMOS, NMOS, CMOS ROM-stand 1K PMOS, NMOS, CMOS PROM-stand 1K PMOS, NMOS, CMOS
Microprogrammed	user microprogram
DMA	yes
Bus Sizes	max I/O channels 16 (8 bits)
Data Path Width	16 bits
Address Path Width	separate 16 bits
Interrupt	multi-level
Power Requirements	
Timing Requirements	

Manufacturer.....	Teledyne
Model Number.....	TDY-52A-Intel MCS-4
Major Application.....	demo
Data Acquisition-Control..	no
Data Communications.....	no
Human Interface Equipment.	no
Computational.....	no
Other.....	
Availability.....	
First Shipped.....	2/74 4 shipped
Cost.....	$995-$1,895
Technology.....	PMOS
Chip-Set Family Size.....	40 chips/2 x 2" board (hybrid)
Architecture.....	4 bit PMOS
Chips In CPU/Pins.....	1 chip/16 pins
Peripheral Interfaces.....	
Special Purpose Chips.....	
Software.....	bundled
Resident Assembler.....	no
Cross Assembler.....	yes
Monitor.....	no
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	10.8usec (4 bits)
Number of Instructions....	46 (8 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary/decimal
Memory Requirements.....	RAM-stand 2K bits PMOS ROM-stand 64K bits bipolar PROM-stand 32K bits PMOS
Microprogrammed.....	no
DMA.....	no
Bus Sizes.....	max I/O channels 8 (4-32 bits)
Data Path Width.....	4 bits
Address Path Width.....	shared with memory
Interrupt.....	yes
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Teledyne
Model Number	TDY-52B-National MM5750
Major Application	military systems
Data Acquisition-Control	intelligent terminals
Data Communications	no
Human Interface Equipment	no
Computational	process controller
Other	
Availability	
First Shipped	10/74
Cost	$995-$.,895
Technology	PMOS
Chip-Set Family Size	44 chips/2 x 2" board (hybrid)
Architecture	4 bit PMOS
Chips In CPU/Pins	6 chips/24 pins
Peripheral Interfaces	
Special Purpose Chips	
Software	bundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	4.55usec (16 bits)
Number of Instructions	60 (16, 32 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand NMOS, CMOS ROM-stand 64K bits bipolar PROM-stand 64K bits bipolar
Microprogrammed	user microprogram
DMA	yes
Bus Sizes	max I/O channels 64 (16 bits)
Data Path Width	4 bits
Address Path Width	shared with memory
Interrupt	vectored
Power Requirements	
Timing Requirements	

Manufacturer	Three Phoenix
Model Number	-- Intel 8008
Major Application	intelligent terminals
Data Acquisition-Control	intelligent terminals
Data Communications	no
Human Interface Equipment	no
Computational	no
Other	
Availability	Double Sourced
First Shipped	11/73 100 shipped
Cost	$995-$1,500
Technology	PMOS
Chip-Set Family Size	58-60 chips/14 x 7" board
Architecture	8 bit PMOS
Chips In CPU/Pins	1 chip/18 pins
Peripheral Interfaces	
Special Purpose Chips	
Software	unbundled
Resident Assembler	yes
Cross Assembler	yes
Monitor	no
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	20usec (8 bits)
Number of Instructions	47 (8 bits)
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	internal code-binary
Memory Requirements	RAM-stand 8K bits NMOS ROM-stand 24K bits PMOS PROM-stand 24K bits PMOS
Microprogrammed	no
DMA	yes
Bus Sizes	max I/O channels 16 (8 bits)
Data Path Width	8 bits
Address Path Width	shared with memory
Interrupt	no
Power Requirements	
Timing Requirements	

Manufacturer.....	Varitel
Model Number.....	MC-8-Intel 8008
Major Application.....	synchronizer
Data Acquisition-Control..	no
Data Communications.....	peripheral controller
Human Interface Equipment.	no
Computational.....	process controller
Other.....	
Availability.....	
First Shipped.....	4/74 12 shipped
Cost.....	$315-$800
Technology.....	PMOS
Chip-Set Family Size.....	31-86 chips/12 x 9.5" board
Architecture.....	8 bit PMOS
Chips In CPU/Pins.....	1 chip/18 pins
Peripheral Interfaces.....	tty, display
Special Purpose Chips.....	
Software.....	unbundled
Resident Assembler.....	yes
Cross Assembler.....	no
Monitor.....	yes
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	20usec (8 bits)
Number of Instructions....	48 (8, 16, 24 bits)
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	internal code-binary
Memory Requirements.....	RAM-stand 8-32K bits NMOS ROM- PROM-stand 2-8K bits PMOS
Microprogrammed.....	no
DMA.....	yes
Bus Sizes.....	max I/O channels 32 (8 bits)
Data Path Width.....	8 bits
Address Path Width.....	shared with memory
Interrupt.....	8 level vectored
Power Requirements.....	
Timing Requirements.....	

Manufacturer	AMI
Model Number	CK114
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	
Technology	
Chip-Set Family Size	6 CPU chips
Architecture	
Chips In CPU/Pins	16, 28, 40 pins per package
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	yes
Monitor	
High Level Languages	no
Instruction Simulator	yes
Prototyping System	no
Reg. Load Time For Instr.	5usec per bit
Reg to Reg Add Time	
Number of Instructions	75
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	16 condition codes
Memory Requirements	2K words max
Microprogrammed	
DMA	no
Bus Sizes	12 bits
Data Path Width	any number of digits
Address Path Width	12 bits
Interrupt	no
Power Requirements	0, -15, -27
Timing Requirements	200KHz

Manufacturer	Fairchild
Model Number	PPS-24
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	
Technology	
Chip-Set Family Size	7 CPU chips
Architecture	
Chips In CPU/Pins	16, 18, 24, 40 pins/package
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	yes
Monitor	
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	62.5usec per word
Reg to Reg Add Time	
Number of Instructions	46
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	2 condition codes
Memory Requirements	6656 words max
Microprogrammed	
DMA	no
Bus Sizes	12 bits
Data Path Width	25 digits max
Address Path Width	
Interrupt	no
Power Requirements	5, 0, -10
Timing Requirements	400KHz

Manufacturer	Intel
Model Number	MCS-4
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	
Technology	
Chip-Set Family Size	1 CPU chip
Architecture	
Chips In CPU/Pins	16 pins per package
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	
High Level Languages	yes
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	10.8usec
Reg to Reg Add Time	
Number of Instructions	45
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	4 condition codes
Memory Requirements	4K words max
Microprogrammed	
DMA	no
Bus Sizes	8 bits
Data Path Width	4 bits max
Address Path Width	
Interrupt	no
Power Requirements	0, -15
Timing Requirements	75KHz

Manufacturer.....	Intel
Model Number.....	MCS-8
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	
Cost.....	
Technology.....	
Chip-Set Family Size.....	1 CPU chip
Architecture.....	
Chips In CPU/Pins.....	18 pins per package
Peripheral Interfaces.....	
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	
High Level Languages.....	yes
Instruction Simulator.....	yes
Prototyping System.....	yes
Reg. Load Time For Instr..	7.5usec
Reg to Reg Add Time.....	
Number of Instructions....	48
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	4 condition codes
Memory Requirements.....	16K words max
Microprogrammed.....	
DMA.....	yes
Bus Sizes.....	8 bits
Data Path Width.....	8 bits max
Address Path Width.....	
Interrupt.....	yes
Power Requirements.....	0, 5, -9
Timing Requirements.....	800KHz

Manufacturer	RIC
Model Number	PPS
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	
Technology	
Chip-Set Family Size	5 CPU chips
Architecture	
Chips In CPU/Pins	42 pins per package
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	yes
Monitor	
High Level Languages	no
Instruction Simulator	yes
Prototyping System	yes
Reg. Load Time For Instr.	5usec per bit
Reg to Reg Add Time	
Number of Instructions	50
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	4 condition codes
Memory Requirements	4K words max
Microprogrammed	
DMA	no
Bus Sizes	8 bits
Data Path Width	4 bits
Address Path Width	
Interrupt	no
Power Requirements	0, -17
Timing Requirements	200KHz

Manufacturer.....	Signetics
Model Number.....	PIP
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	
Cost.....	
Technology.....	
Chip-Set Family Size.....	1 CPU chip
Architecture.....	
Chips In CPU/Pins.....	40 pins per package
Peripheral Interfaces.....	
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	no
Cross Assembler.....	yes
Monitor.....	
High Level Languages.....	no
Instruction Simulator.....	yes
Prototyping System.....	yes
Reg. Load Time For Instr..	approx. 5usec
Reg to Reg Add Time.....	
Number of Instructions....	68
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	7 condition codes
Memory Requirements.....	32K words max
Microprogrammed.....	
DMA.....	yes
Bus Sizes.....	8 bits
Data Path Width.....	8 bits
Address Path Width.....	
Interrupt.....	yes
Power Requirements.....	12, 5, 0
Timing Requirements.....	1.1MHz

Manufacturer.....	Control Logic
Model Number.....	M-Series-Intel 8080
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	
Cost.....	$590
Technology.....	
Chip-Set Family Size.....	--/2.5 x 4" board
Architecture.....	
Chips In CPU/Pins.....	
Peripheral Interfaces.....	tty, serial, parallel, digital
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	
Number of Instructions....	
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	
Memory Requirements.....	256-64K any mix of RAM-ROM
Microprogrammed.....	
DMA.....	
Bus Sizes.....	8 bits
Data Path Width.....	4 bits
Address Path Width.....	
Interrupt.....	
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Digital Equipment Corp.
Model Number	LSI-11-Western Digital
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	under $1K
Technology	
Chip-Set Family Size	
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	all DEC peripherals
Special Purpose Chips	
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	
High Level Languages	yes
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	to 32K bits
Microprogrammed	
DMA	
Bus Sizes	16 bits
Data Path Width	16 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	General Automation
Model Number	LSI 12/16
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$635 (1000)
Technology	
Chip-Set Family Size	--/7.75 x 10" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	SPC 16 peripherals
Special Purpose Chips	
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	
High Level Languages	yes
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	1K-32K any mix of RAM-ROM
Microprogrammed	
DMA	
Bus Sizes	12 bits
Data Path Width	16 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer.....	Intel
Model Number.....	Immy-43-Intel 4040
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	
Cost.....	
Technology.....	
Chip-Set Family Size.....	--/8 x 6.18" board
Architecture.....	
Chips In CPU/Pins.....	
Peripheral Interfaces.....	tty
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	yes
Cross Assembler.....	yes
Monitor.....	
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg To Reg Add Time.....	
Number of Instructions....	
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	
Memory Requirements.....	RAM-320 ROM-256K
Microprogrammed.....	
DMA.....	
Bus Sizes.....	8 bits
Data Path Width.....	4 bits
Address Path Width.....	
Interrupt.....	
Power Requirements.....	
Timing Requirements.....	

Manufacturer	National Semiconductor
Model Number	8C 200-National IMP8
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$800
Technology	
Chip-Set Family Size	--/8.5 x 11" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	tty, card reader
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	yes
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	256 RAM 0-2048 ROM
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	National Semiconductor
Model Number	16 L 304-National IMP16
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	#3950
Technology	
Chip-Set Family Size	
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	tty, card reader
Special Purpose Chips	
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	4K-65K, 0-2048 ROM
Microprogrammed	
DMA	yes
Bus Sizes	16 bits
Data Path Width	16 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	Pro-Log
Model Number	PL8-401-Intel 4004
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$355
Technology	
Chip-Set Family Size	--/4.5 x 6.5" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	RAM 320-1280 ROM 256-1024
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	4 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	Pro-Log
Model Number	PLS-402-Intel 4004
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$470
Technology	
Chip-Set Family Size	--/4.5 x 6.5" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	RAM 320-1280 ROM 256-1536
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	4 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer.....	Pro-Log
Model Number.....	PLS-403-Intel 4004
Major Application.....	
Data Acquisition-Control..	
Data Communications.....	
Human Interface Equipment.	
Computational.....	
Other.....	
Availability.....	
First Shipped.....	
Cost.....	$590
Technology.....	
Chip-Set Family Size.....	--/4.5 x 6.5" board
Architecture.....	
Chips In CPU/Pins.....	
Peripheral Interfaces.....	
Special Purpose Chips.....	
Software.....	
Resident Assembler.....	no
Cross Assembler.....	no
Monitor.....	
High Level Languages.....	no
Instruction Simulator.....	
Prototyping System.....	
Reg. Load Time For Instr..	
Reg to Reg Add Time.....	
Number of Instructions....	
Arithmetic.....	
Logical.....	
Shift/Rotate.....	
Index Group.....	
Stack Control.....	
Other.....	
Memory Requirements.....	RAM 320-5120 ROM 256-4096
Microprogrammed.....	
DMA.....	
Bus Sizes.....	8 bits
Data Path Width.....	4 bits
Address Path Width.....	
Interrupt.....	
Power Requirements.....	
Timing Requirements.....	

Manufacturer	Pro-Log
Model Number	MPS-803-Intel 8008-1
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$810
Technology	
Chip-Set Family Size	--/4.5 x 6.5" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	RAM 1K-2K ROM 128-512
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	Pro-Log
Model Number	MPS-805-Intel 8008-1
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$980
Technology	
Chip-Set Family Size	--/4.5 x 6.5" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	
Special Purpose Chips	
Software	
Resident Assembler	no
Cross Assembler	no
Monitor	
High Level Languages	no
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	RAM 1K-3K ROM 128-1024
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	8 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

Manufacturer	Warner & Swasey
Model Number	Comstar 4-Intel 4004
Major Application	
Data Acquisition-Control	
Data Communications	
Human Interface Equipment	
Computational	
Other	
Availability	
First Shipped	
Cost	$915
Technology	
Chip-Set Family Size	--/6.5 x 4.5" board
Architecture	
Chips In CPU/Pins	
Peripheral Interfaces	tty, DAC, ADC, floppy, cardread
Special Purpose Chips	tape, printer
Software	
Resident Assembler	yes
Cross Assembler	yes
Monitor	
High Level Languages	yes
Instruction Simulator	
Prototyping System	
Reg. Load Time For Instr.	
Reg to Reg Add Time	
Number of Instructions	
Arithmetic	
Logical	
Shift/Rotate	
Index Group	
Stack Control	
Other	
Memory Requirements	RAM 320-2560 x 4 ROM 1K-4K x 8
Microprogrammed	
DMA	
Bus Sizes	8 bits
Data Path Width	4 bits
Address Path Width	
Interrupt	
Power Requirements	
Timing Requirements	

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	*square metre*	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto*	h
10 = 10^{1}	deka*	da
0.1 = 10^{-1}	deci*	d
0.01 = 10^{-2}	centi*	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

* To be avoided where possible.

MISSION
of
Rome Air Development Center

RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C^3) activities, and in the C^3 areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

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